



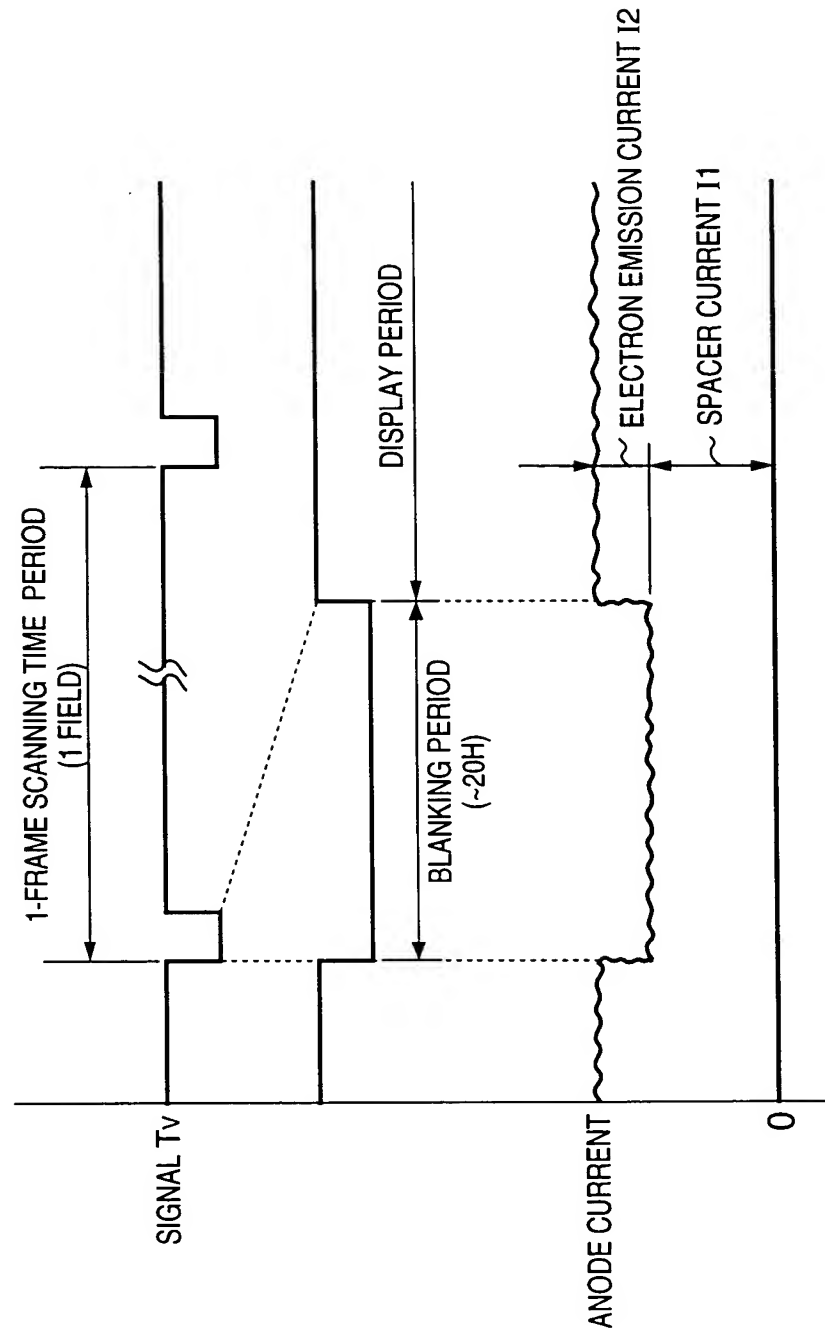
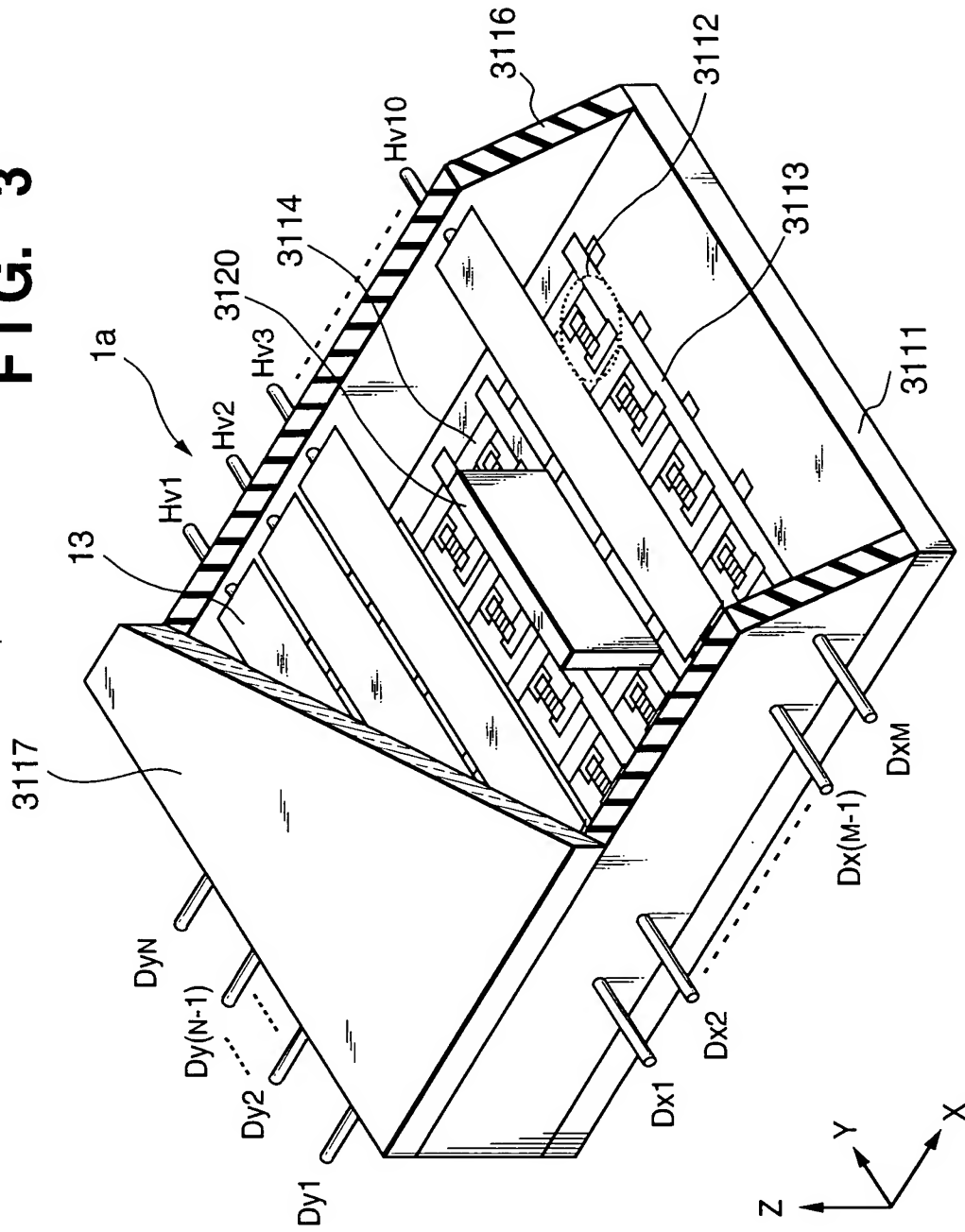
**FIG. 2**

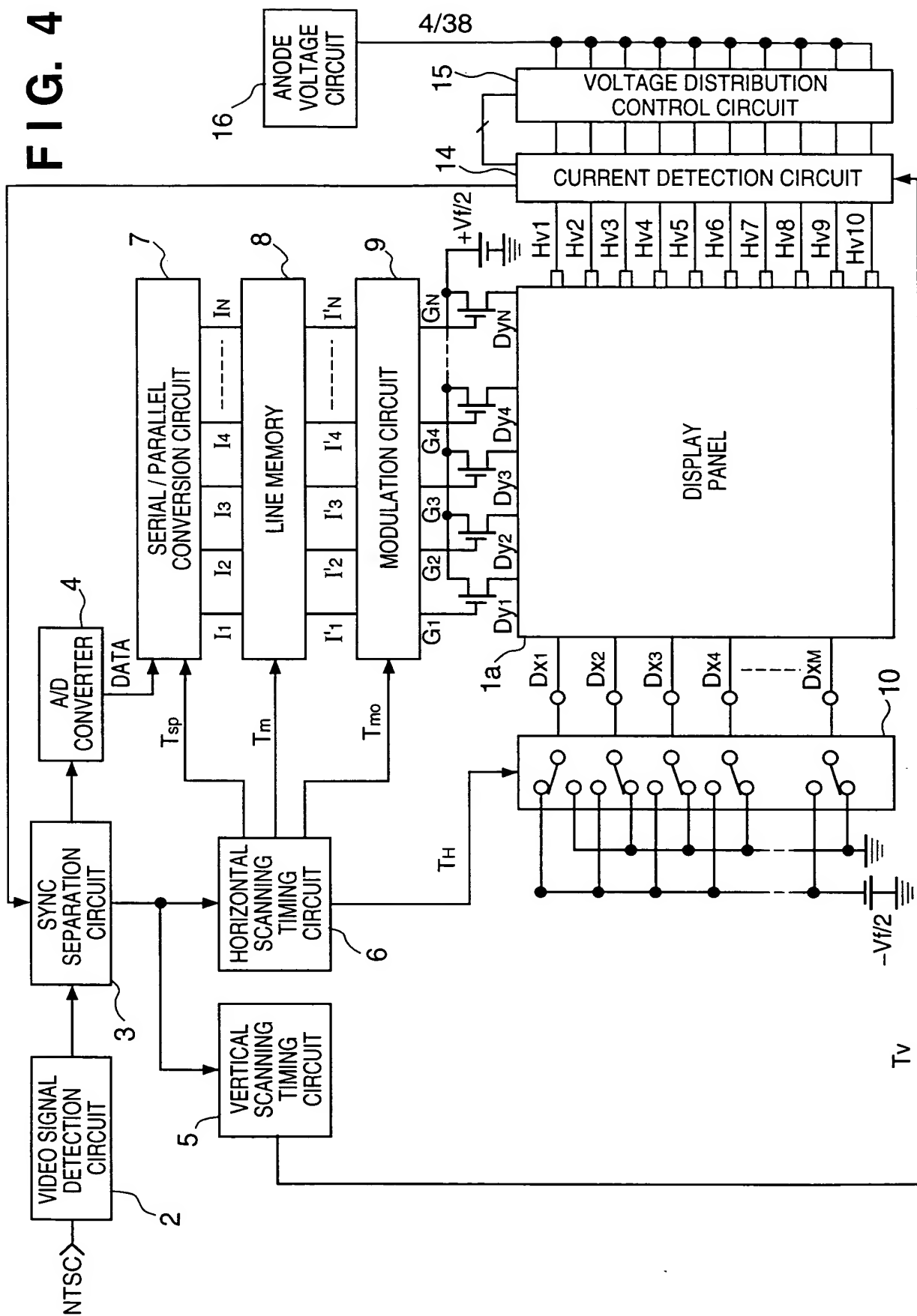
FIG. 3



# FIG. 4

The diagram illustrates a video signal processing system for a color display panel. The system components and their interconnections are as follows:

- Input:** An NTSC video signal is input to the **VIDEO SIGNAL DETECTION CIRCUIT (2)**.
- Timing and Sync Processing:**
  - The **VIDEO SIGNAL DETECTION CIRCUIT (2)** outputs a sync signal to the **SYNC SEPARATION CIRCUIT (3)**.
  - The **SYNC SEPARATION CIRCUIT (3)** outputs a sync signal to the **A/D CONVERTER (4)** and a timing signal to the **HORIZONTAL SCANNING TIMING CIRCUIT (6)**.
  - The **HORIZONTAL SCANNING TIMING CIRCUIT (6)** outputs a timing signal  $T_{sp}$  to the **SERIAL / PARALLEL CONVERSION CIRCUIT (7)** and a timing signal  $T_m$  to the **LINE MEMORY (8)**.
  - The **LINE MEMORY (8)** outputs a timing signal  $T_{mo}$  to the **MODULATION CIRCUIT (9)**.
  - The **MODULATION CIRCUIT (9)** outputs a timing signal  $T_v$  to the **VERTICAL SCANNING TIMING CIRCUIT (5)**.
- Signal Conversion and Memory:**
  - The **A/D CONVERTER (4)** outputs **DATA** to the **SERIAL / PARALLEL CONVERSION CIRCUIT (7)**.
  - The **SERIAL / PARALLEL CONVERSION CIRCUIT (7)** outputs data signals  $I_1, I_2, I_3, I_4, \dots, I_N$  to the **LINE MEMORY (8)**.
  - The **LINE MEMORY (8)** outputs data signals  $I'_1, I'_2, I'_3, I'_4, \dots, I'_N$  to the **MODULATION CIRCUIT (9)**.
- Display Panel and Control:**
  - The **MODULATION CIRCUIT (9)** drives the **DISPLAY PANEL (10)** through a set of transistors ( $G_1, G_2, G_3, G_4, \dots, G_N$ ) and capacitors ( $Dy_1, Dy_2, Dy_3, Dy_4, \dots, Dy_N$ ). The panel is also connected to a common line  $G_N$  and a dynamic line  $Dyn$ .
  - The **DISPLAY PANEL (10)** is connected to a **VOLTAGE DISTRIBUTION CONTROL CIRCUIT (14)** and a **CURRENT DETECTION CIRCUIT (15)**.
  - The **VOLTAGE DISTRIBUTION CONTROL CIRCUIT (14)** outputs a control signal  $4/38$  to the **ANODE VOLTAGE CIRCUIT (16)**.
  - The **CURRENT DETECTION CIRCUIT (15)** outputs a control signal  $15$  to the **VOLTAGE DISTRIBUTION CONTROL CIRCUIT (14)**.



# FIG. 5

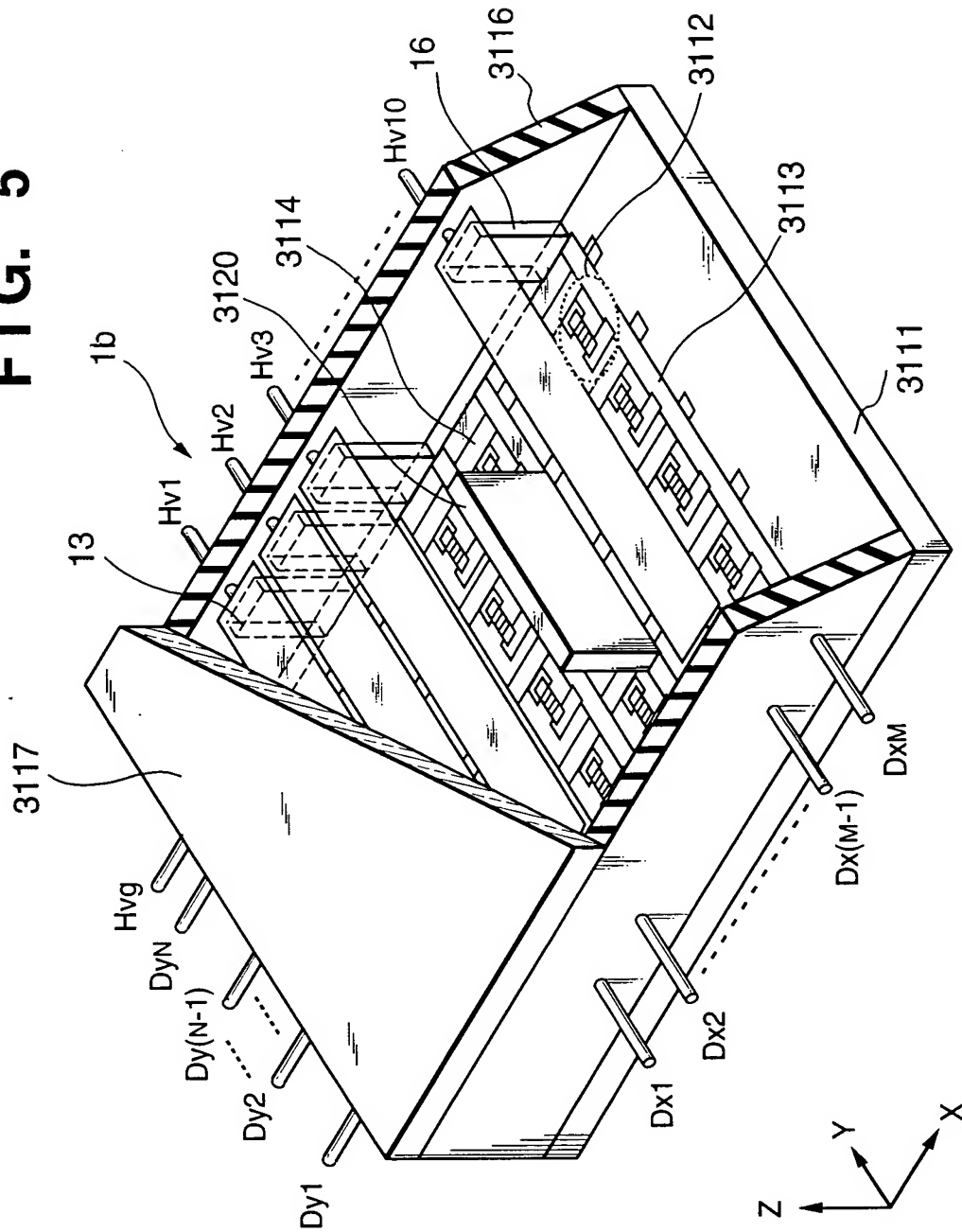
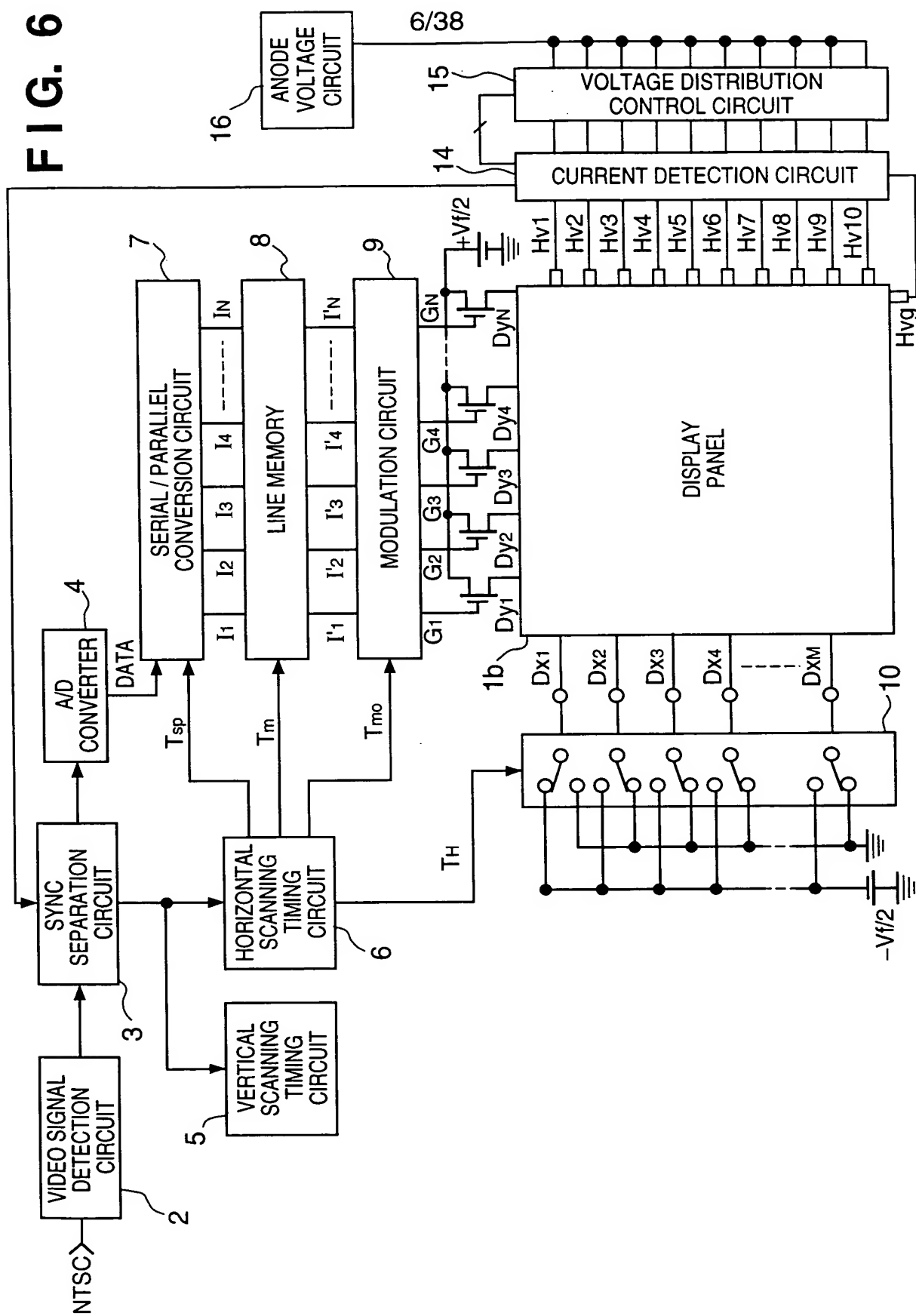
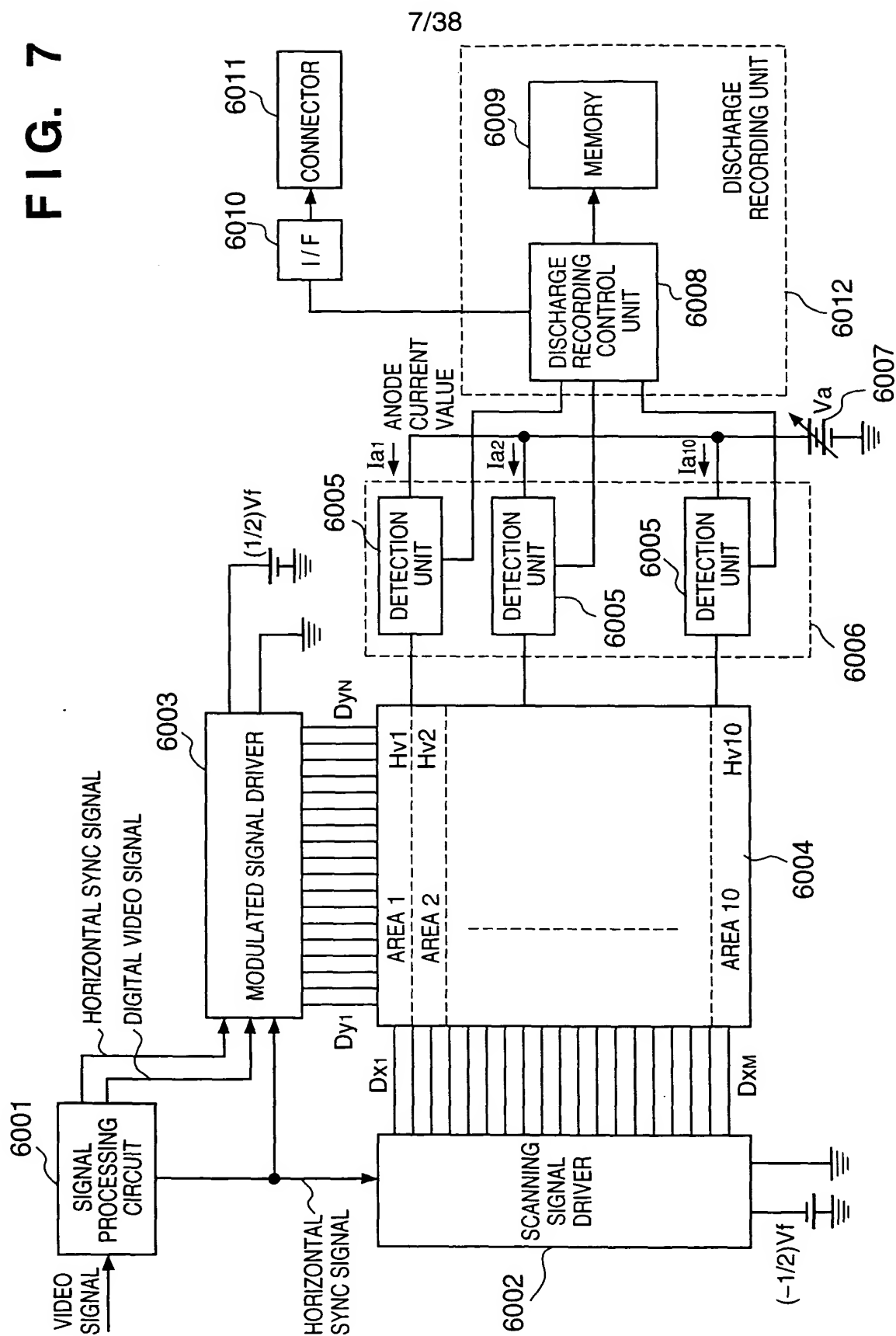


FIG. 6



**FIG. 7**



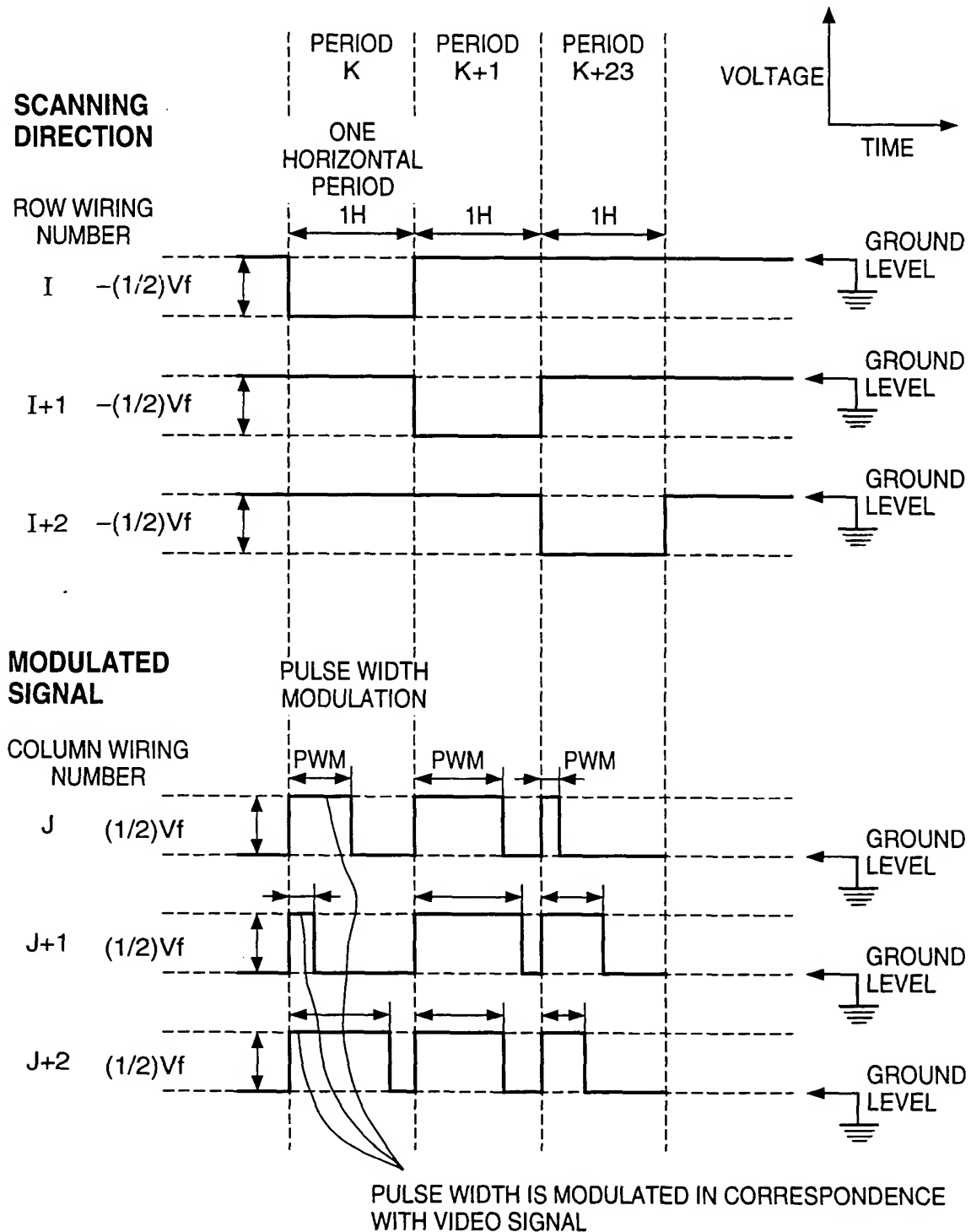
**FIG. 8**



FIG. 9

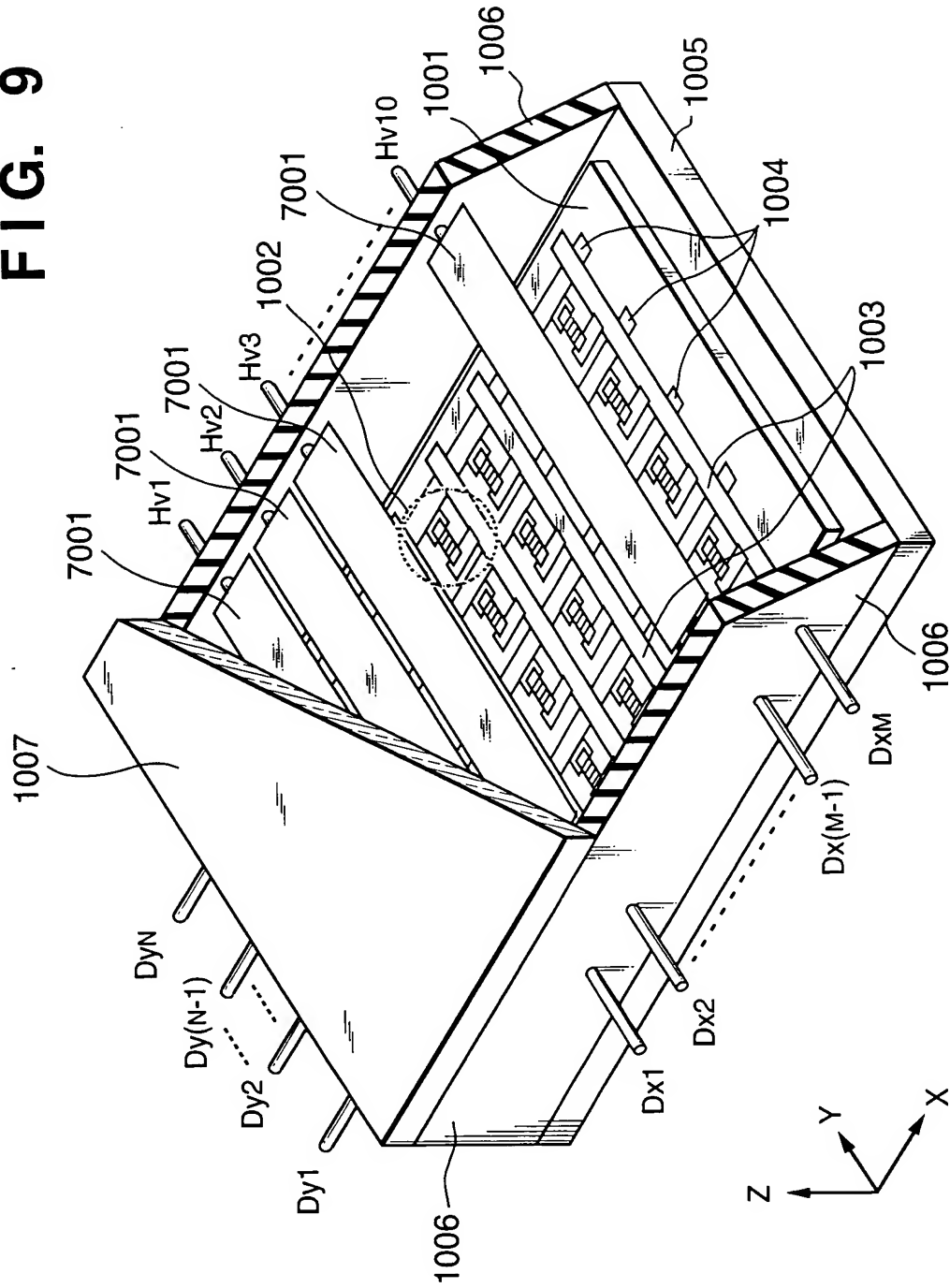


FIG. 10

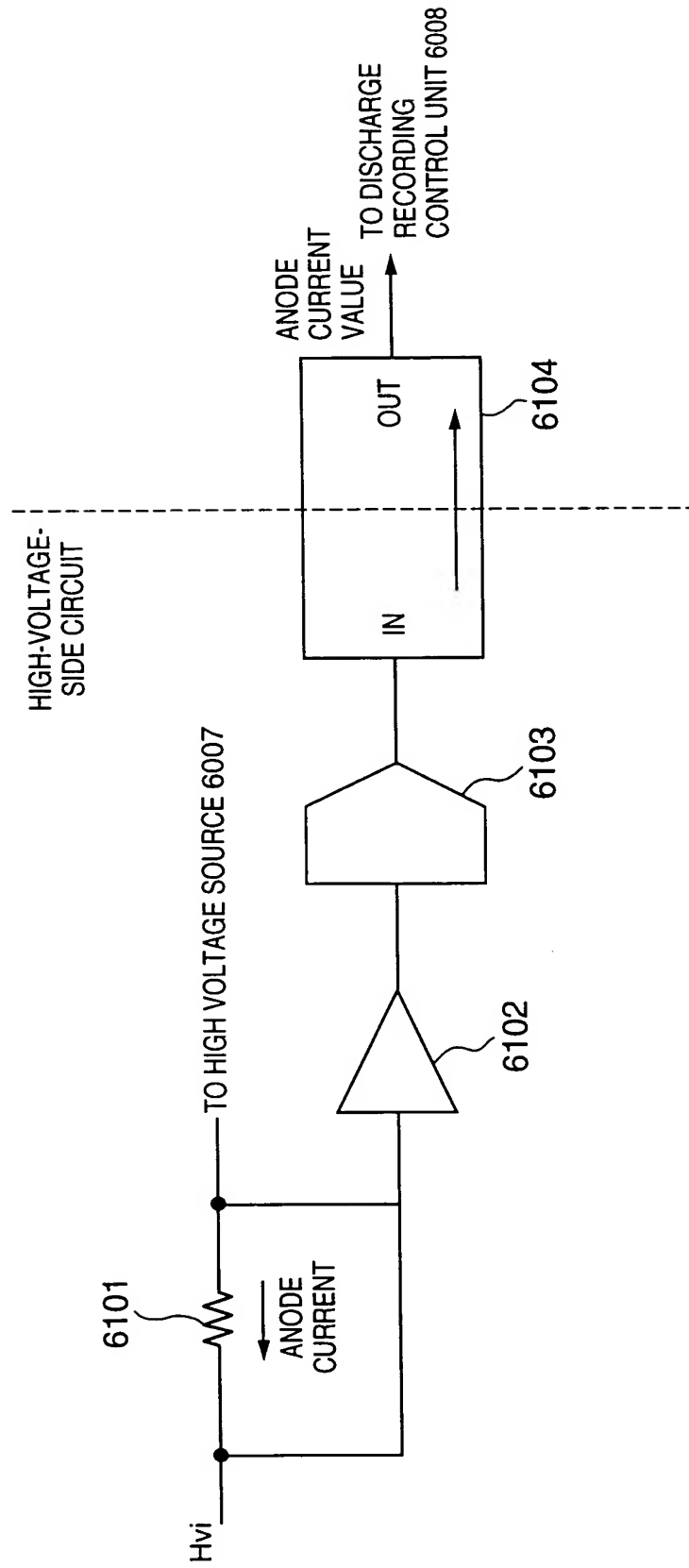


FIG. 11

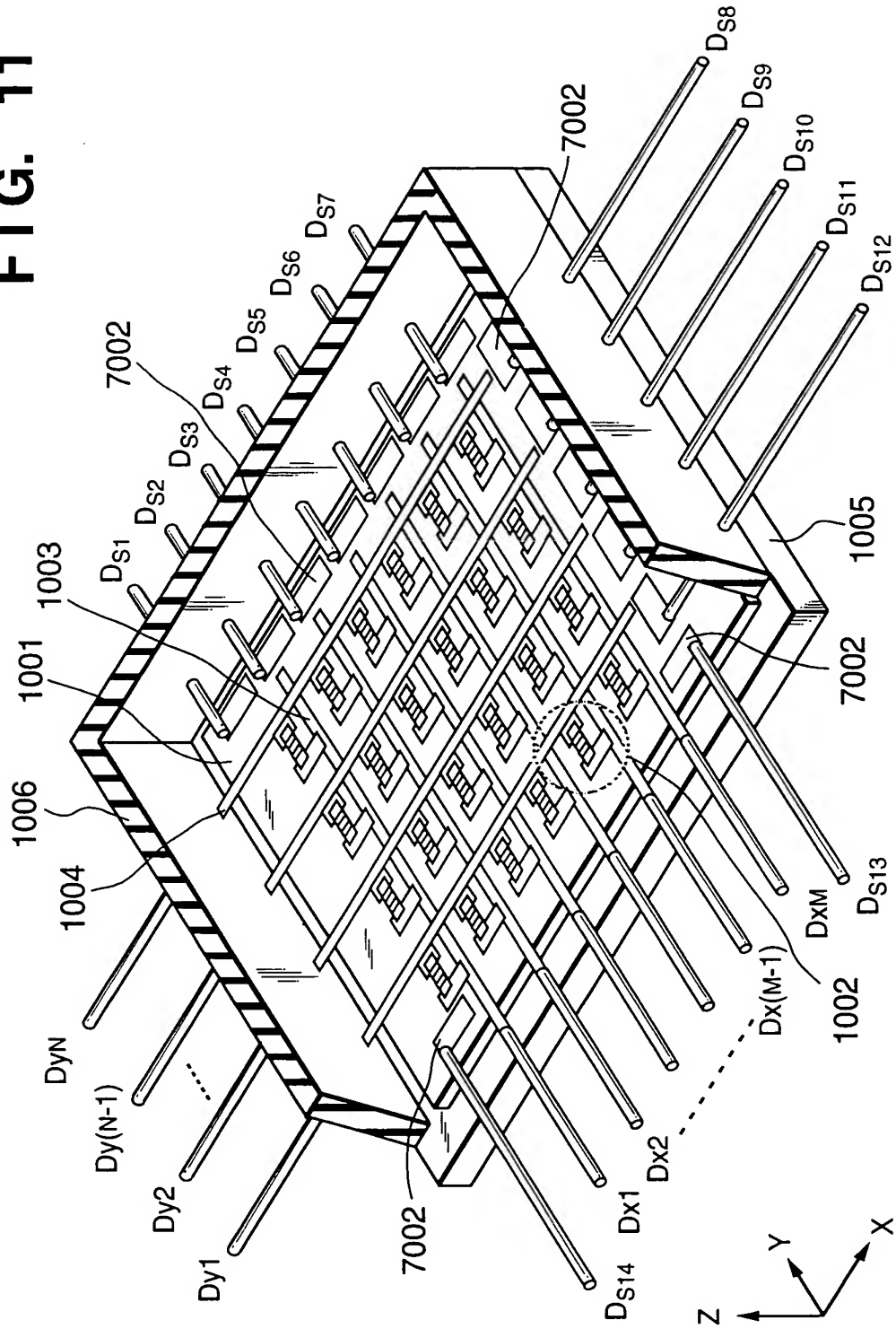
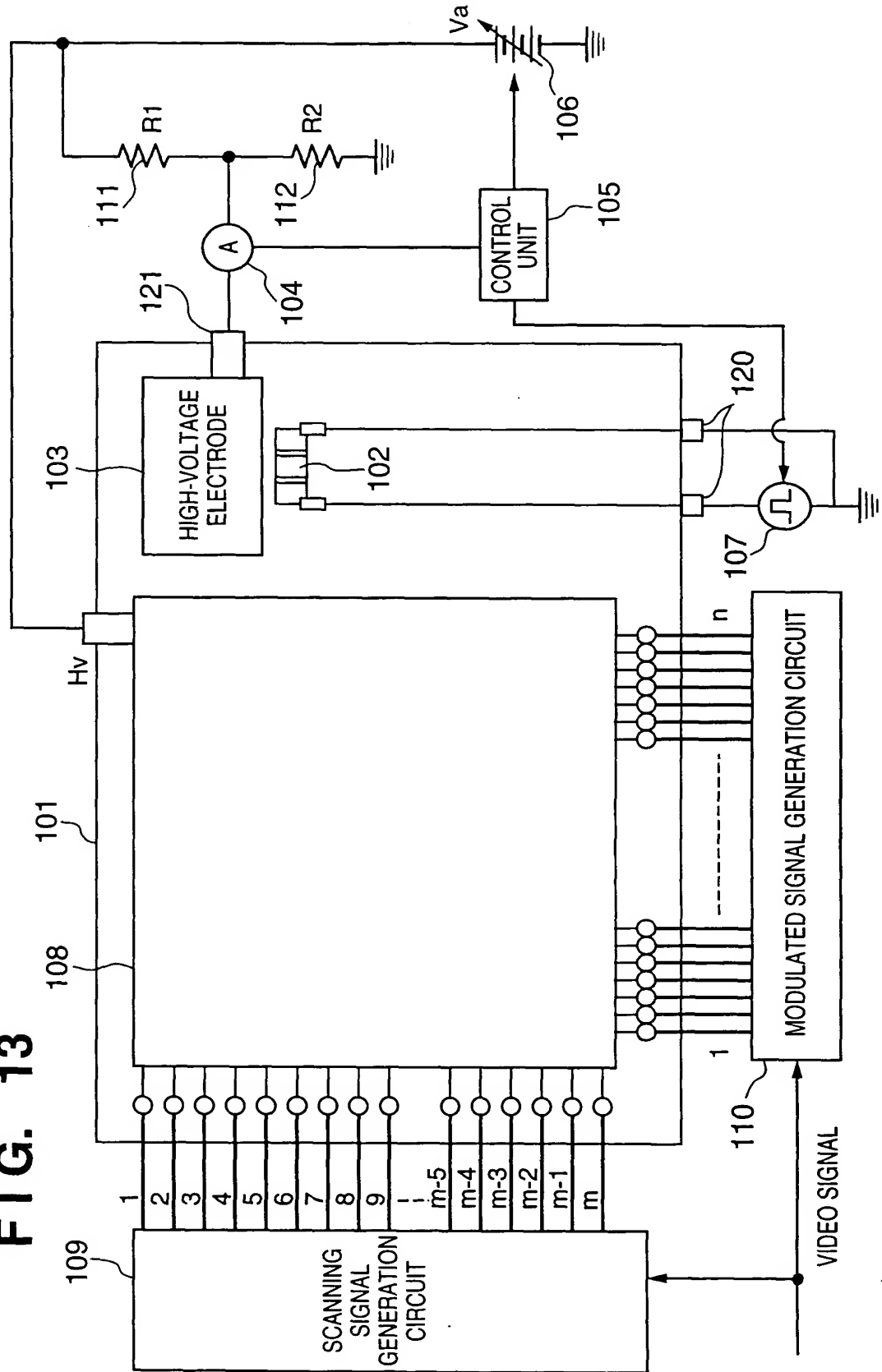




FIG. 13



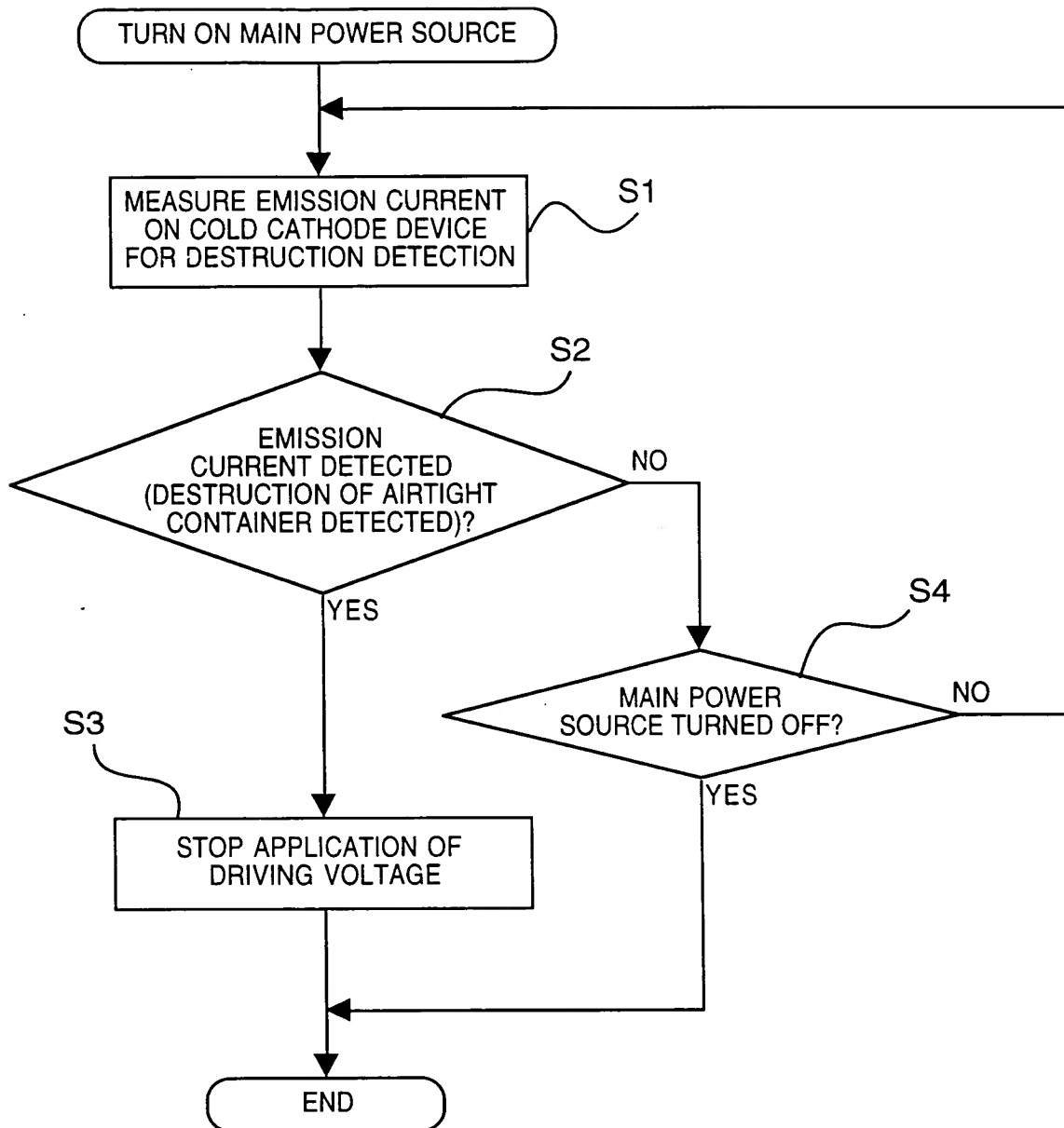
**FIG. 14**

FIG. 15

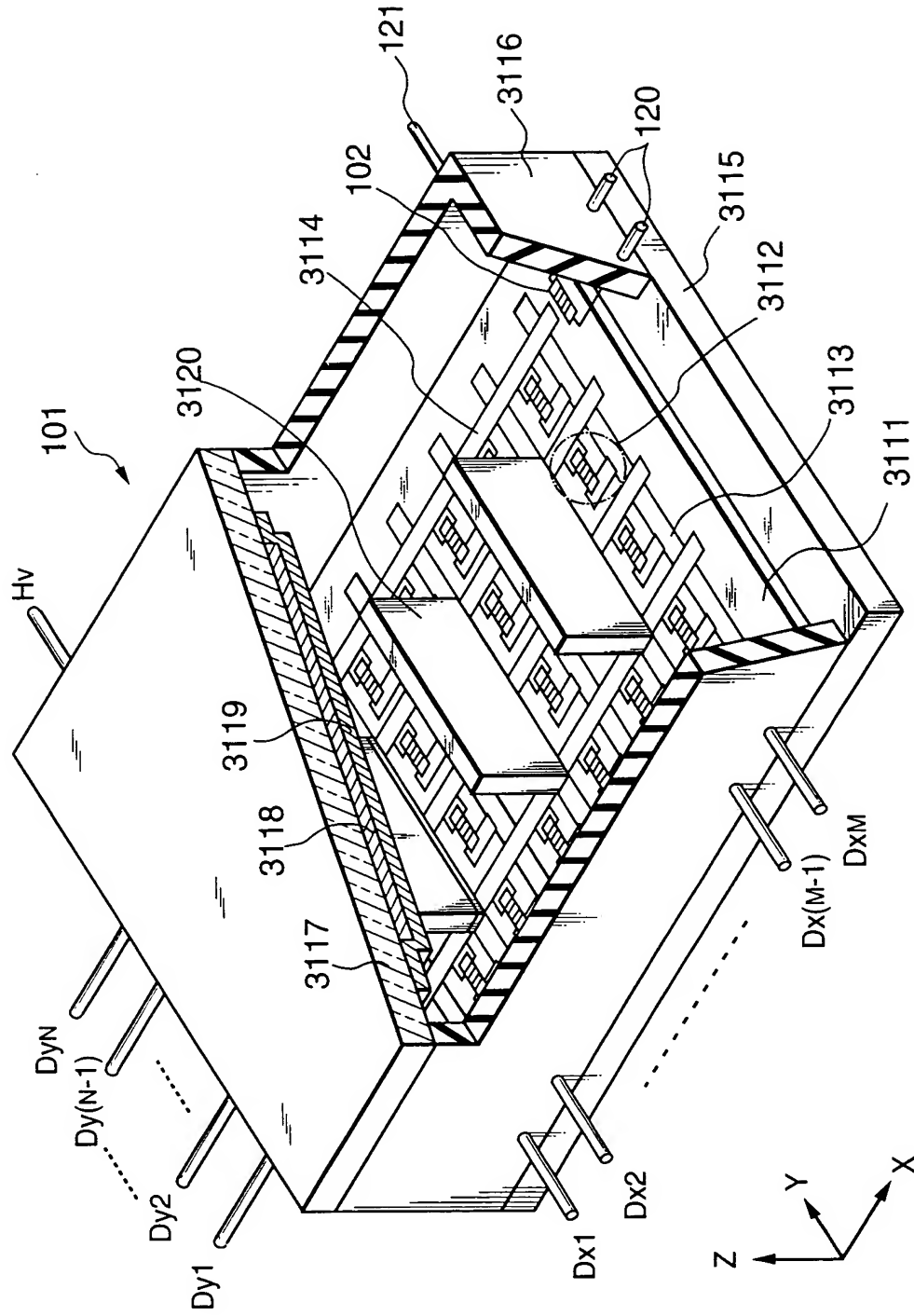


FIG. 16

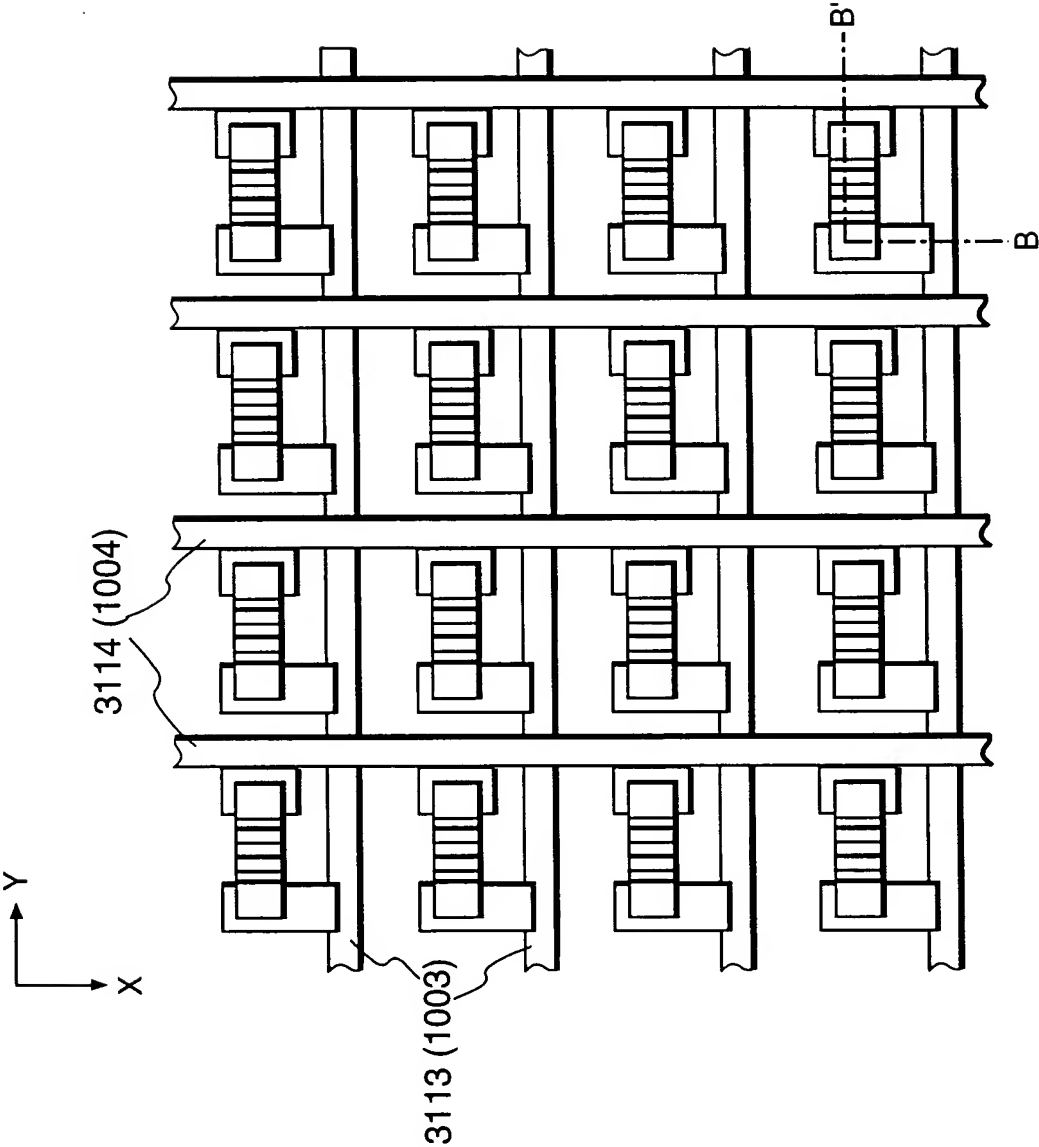
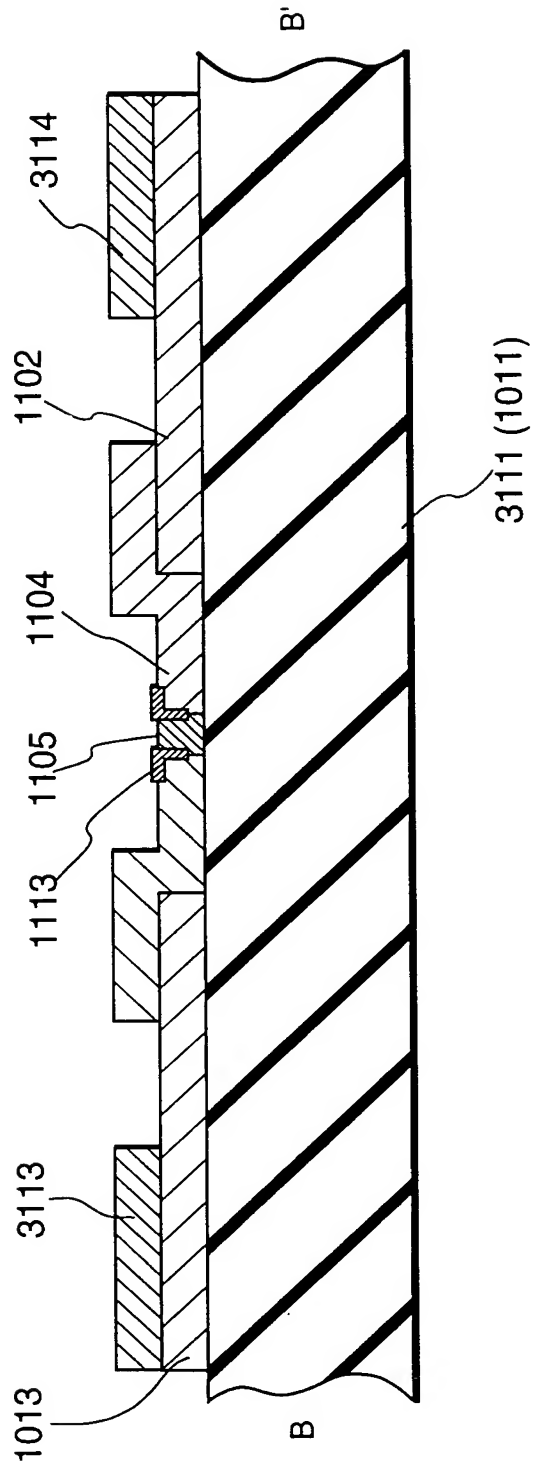
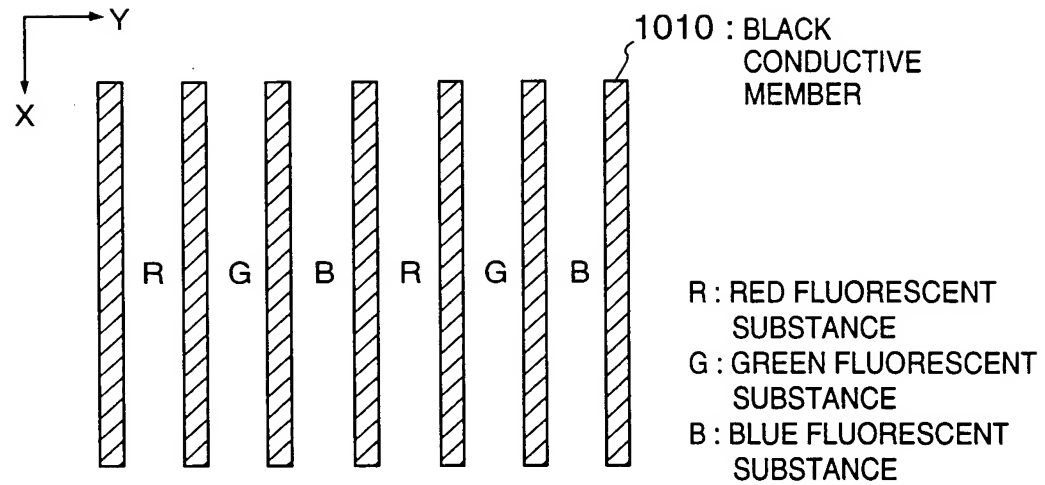
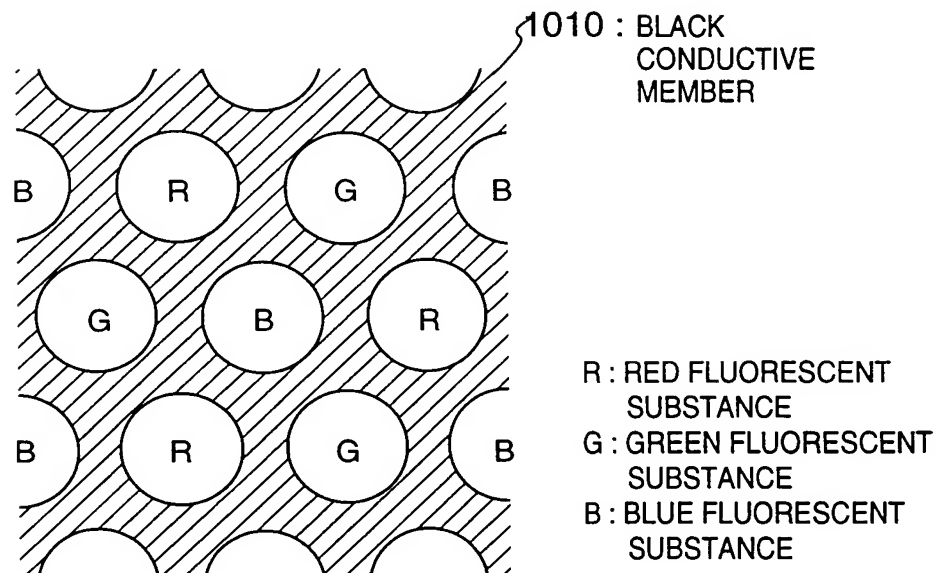


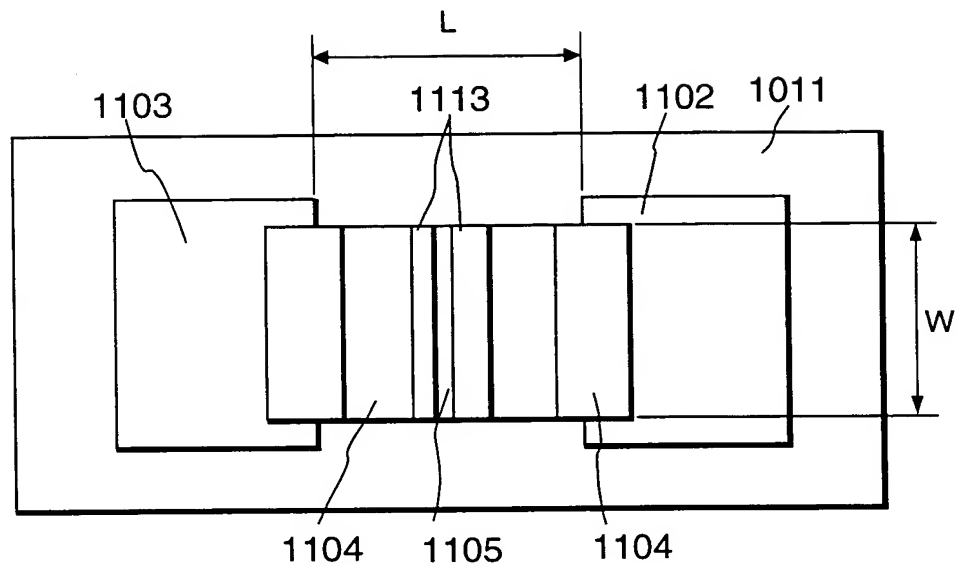


FIG. 17

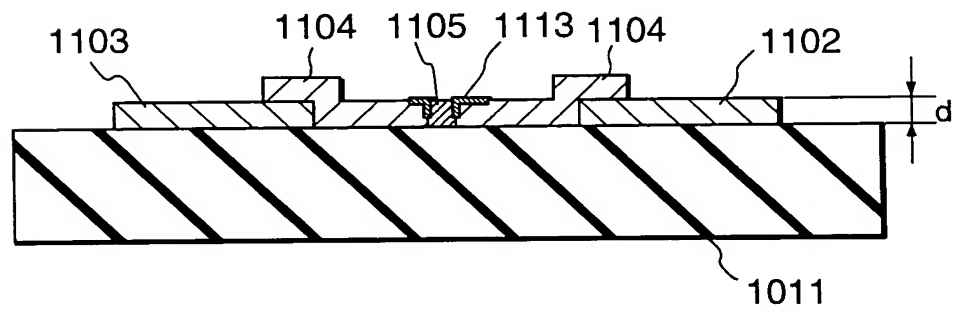


**FIG. 18A****FIG. 18B**

**FIG. 19A**



**FIG. 19B**



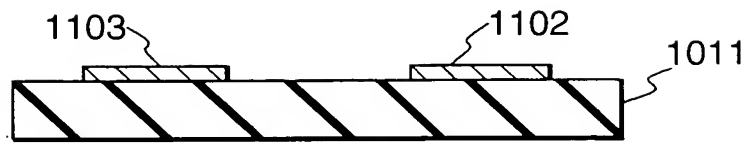
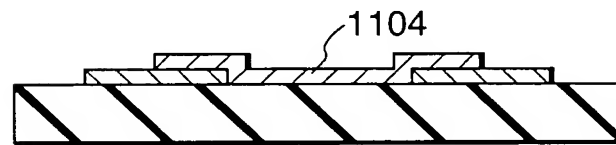
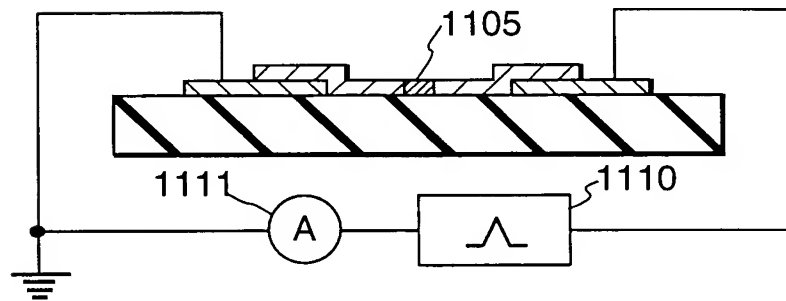
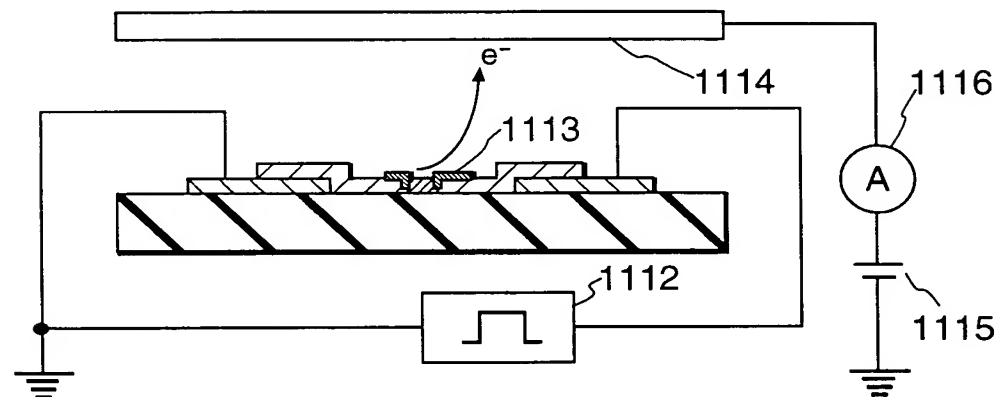
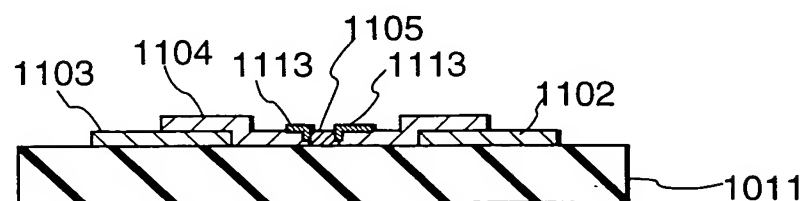
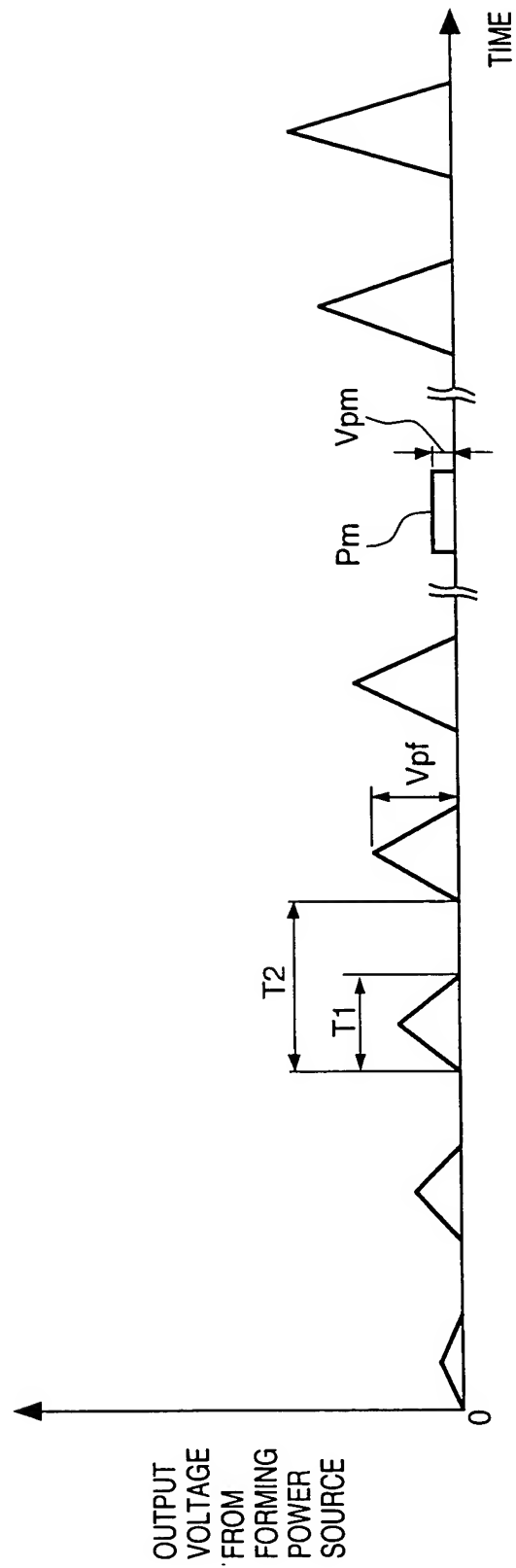
**FIG. 20A****FIG. 20B****FIG. 20C****FIG. 20D****FIG. 20E**

FIG. 21



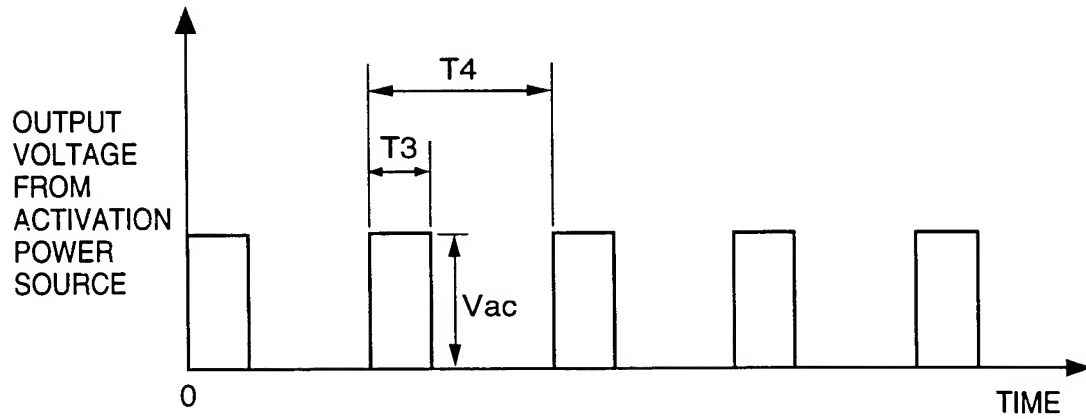
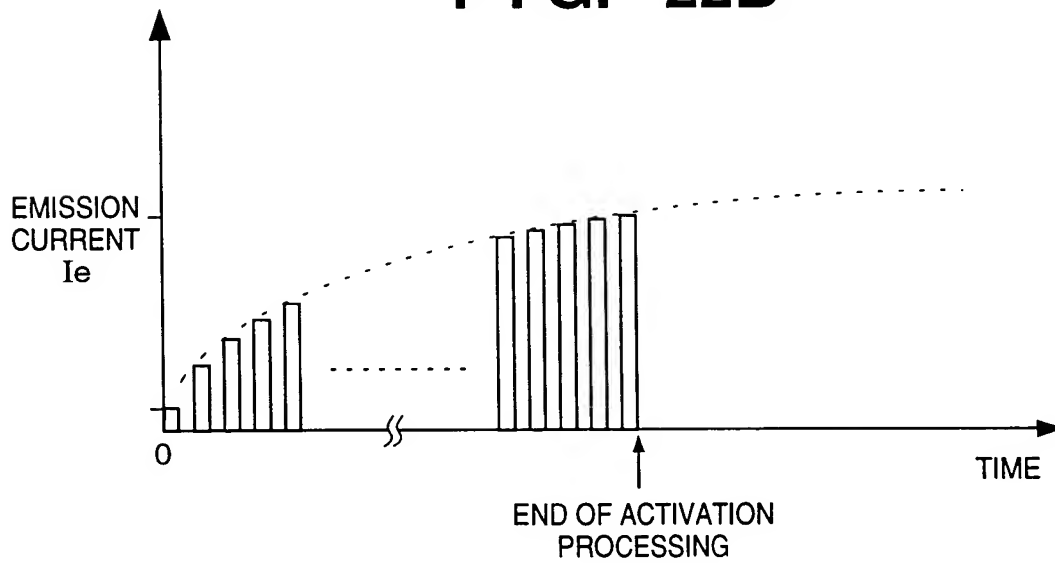
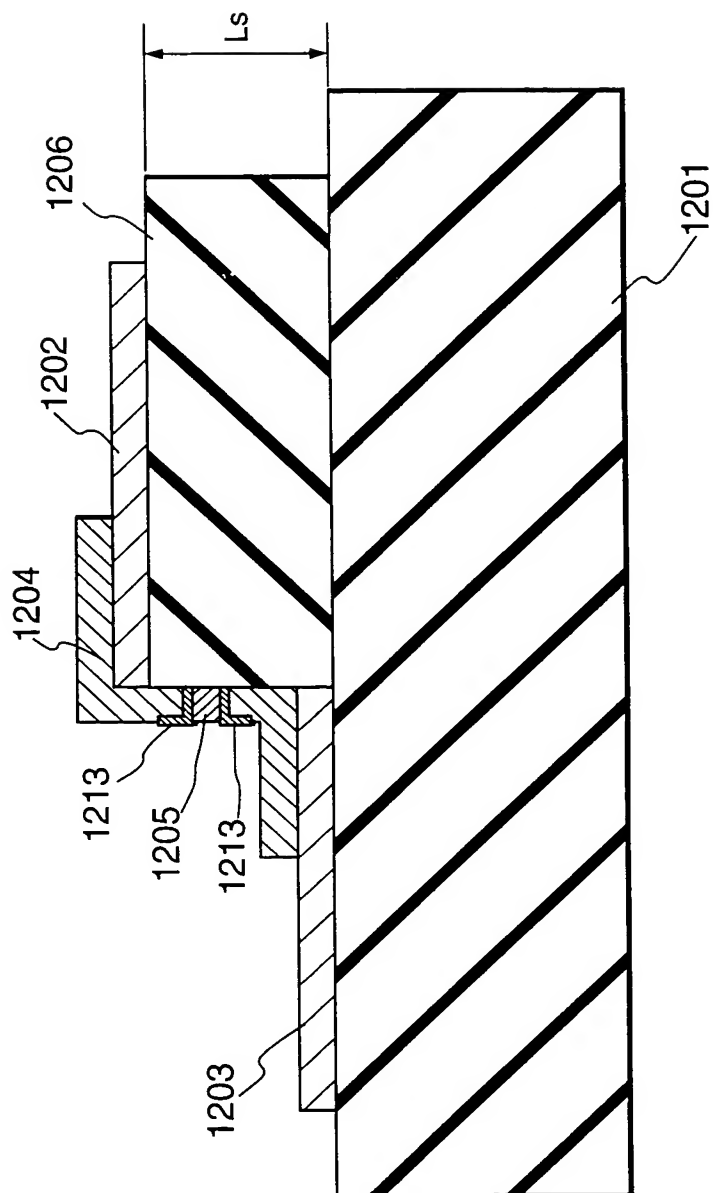
**FIG. 22A****FIG. 22B**

FIG. 23



24/38

FIG. 24A

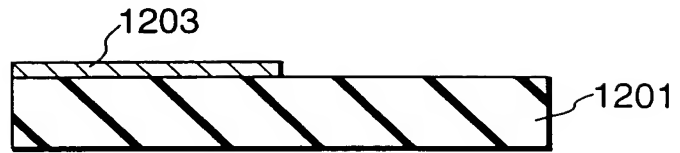


FIG. 24B

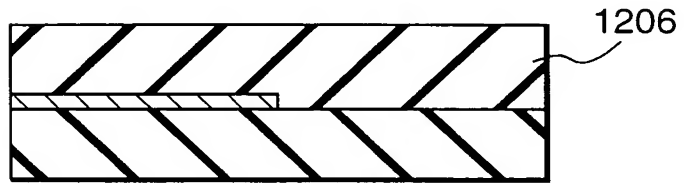


FIG. 24C

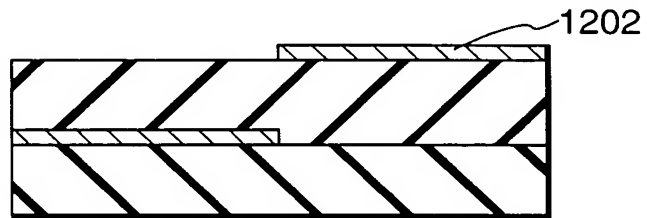


FIG. 24D

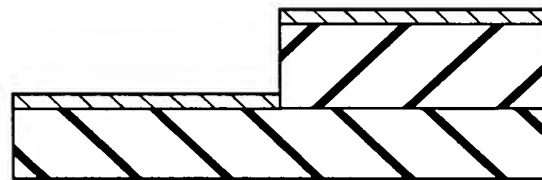


FIG. 24E

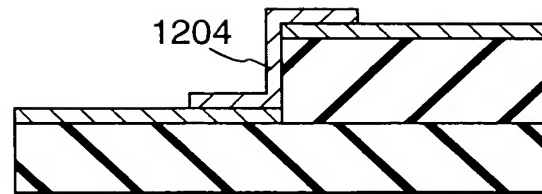
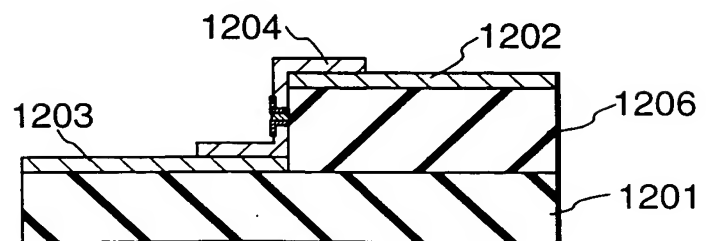


FIG. 24F





**FIG. 25**

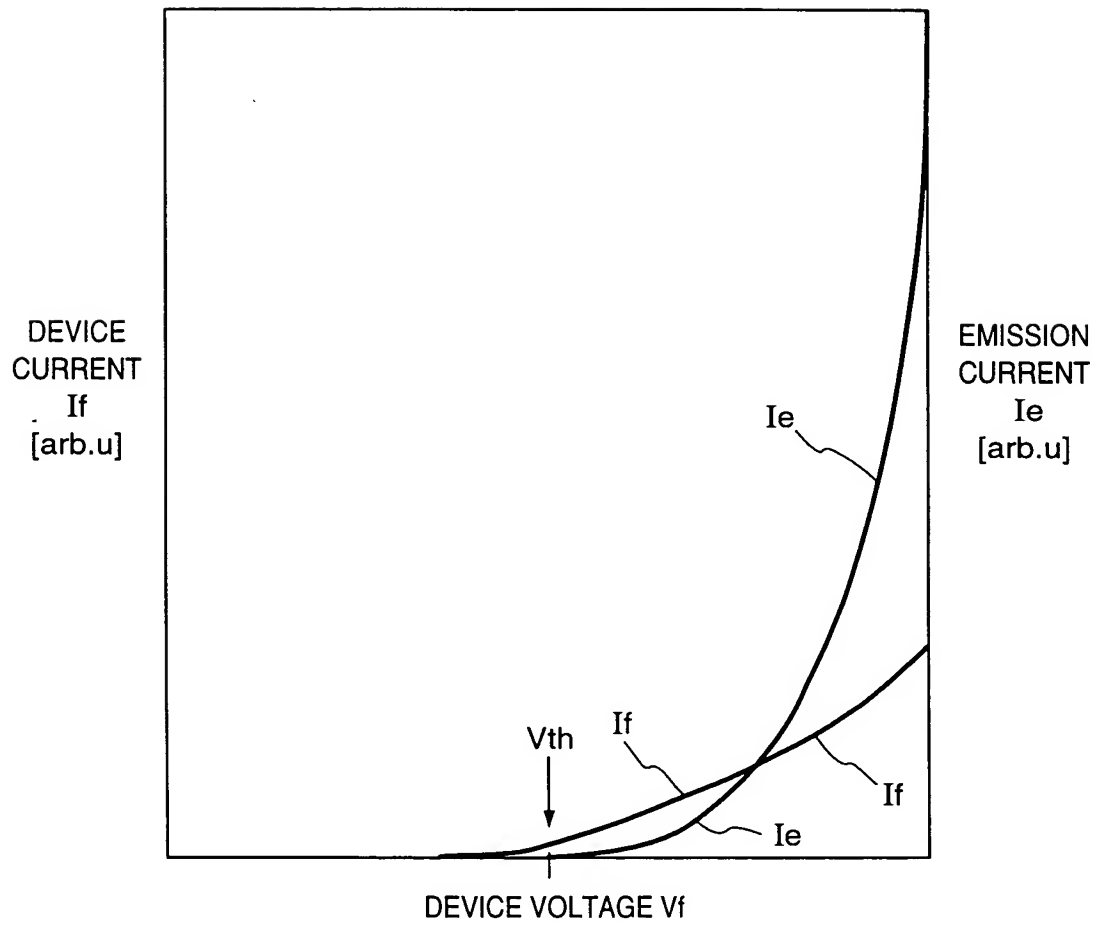
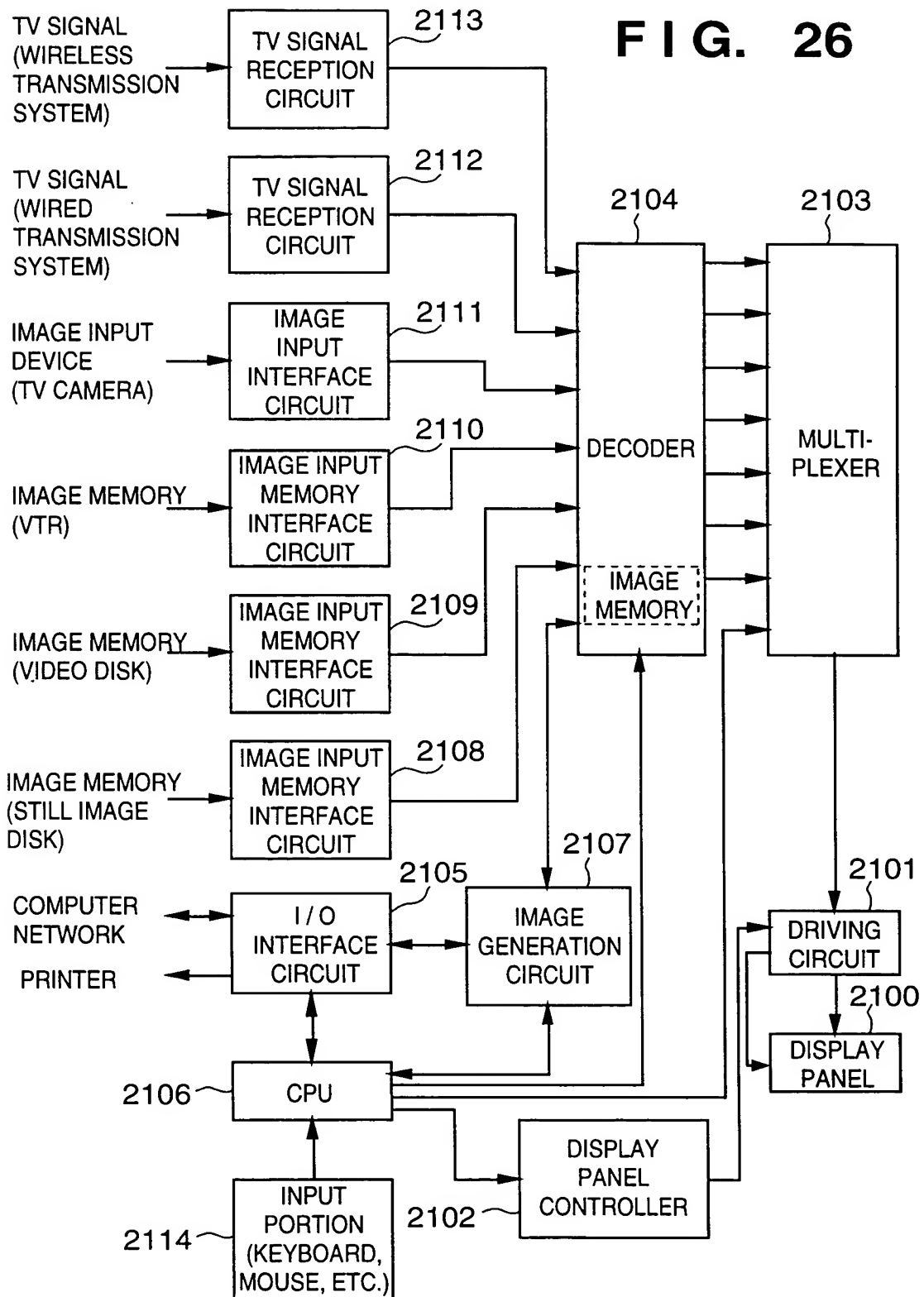
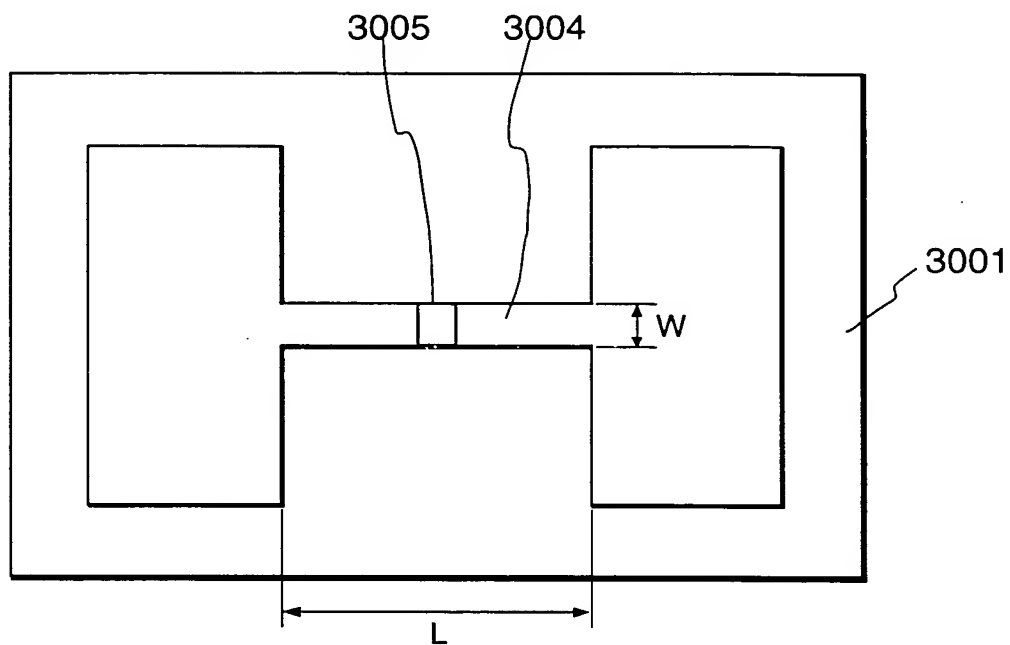
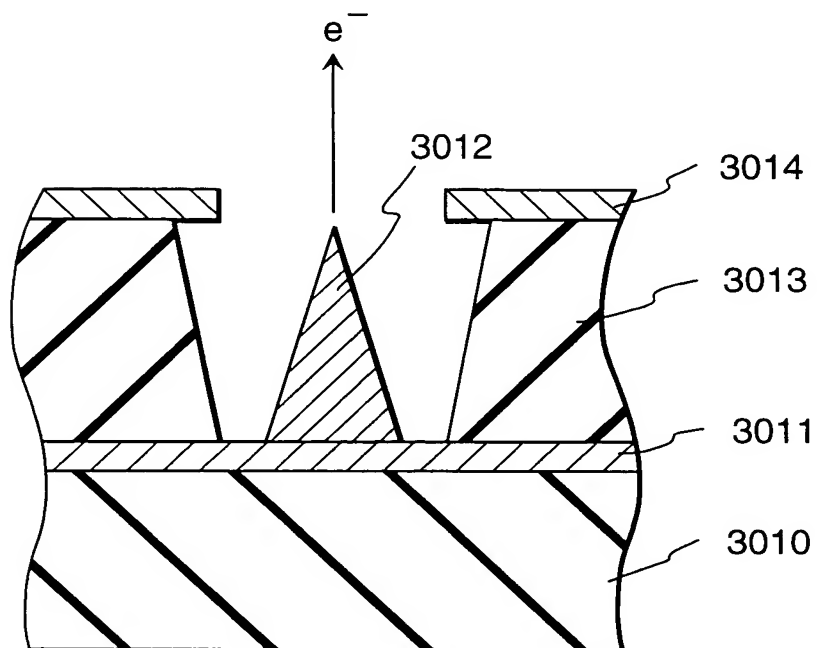


FIG. 26



**FIG. 27****FIG. 28**

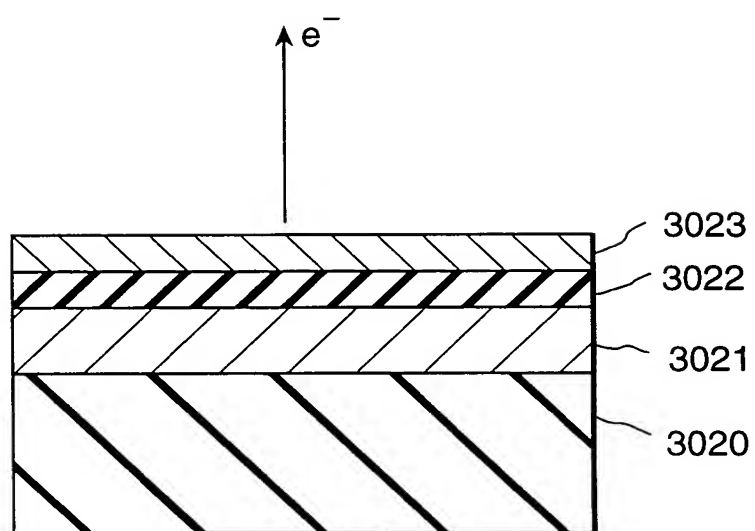
**FIG. 29**

FIG. 30

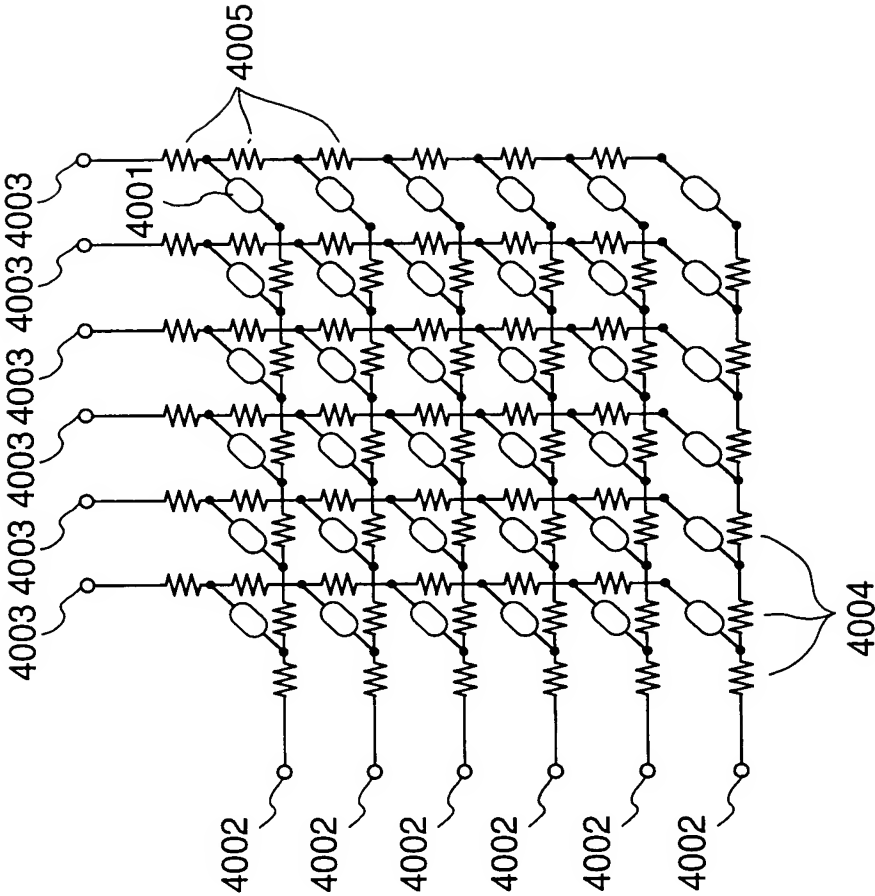


FIG. 31

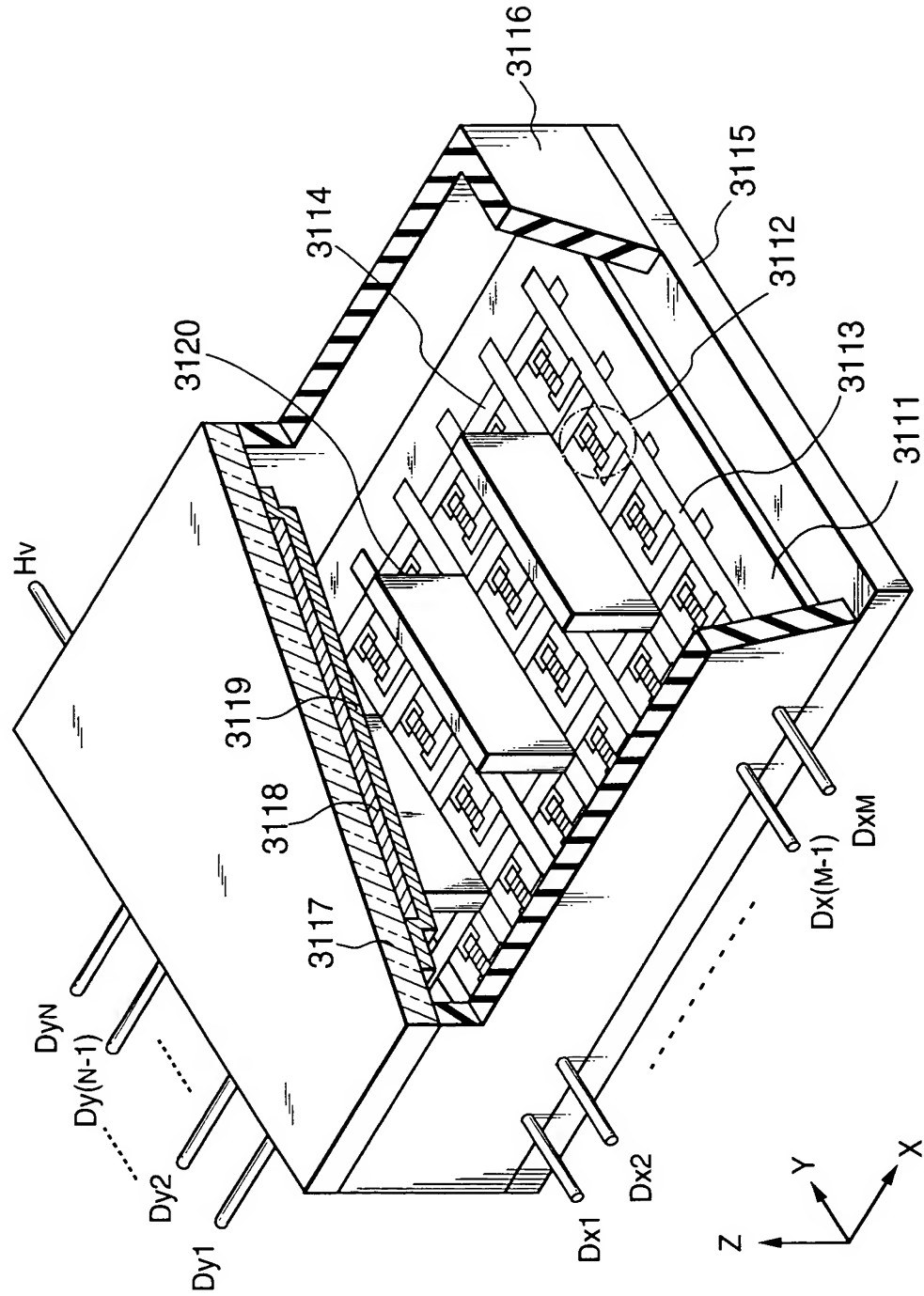


FIG. 32

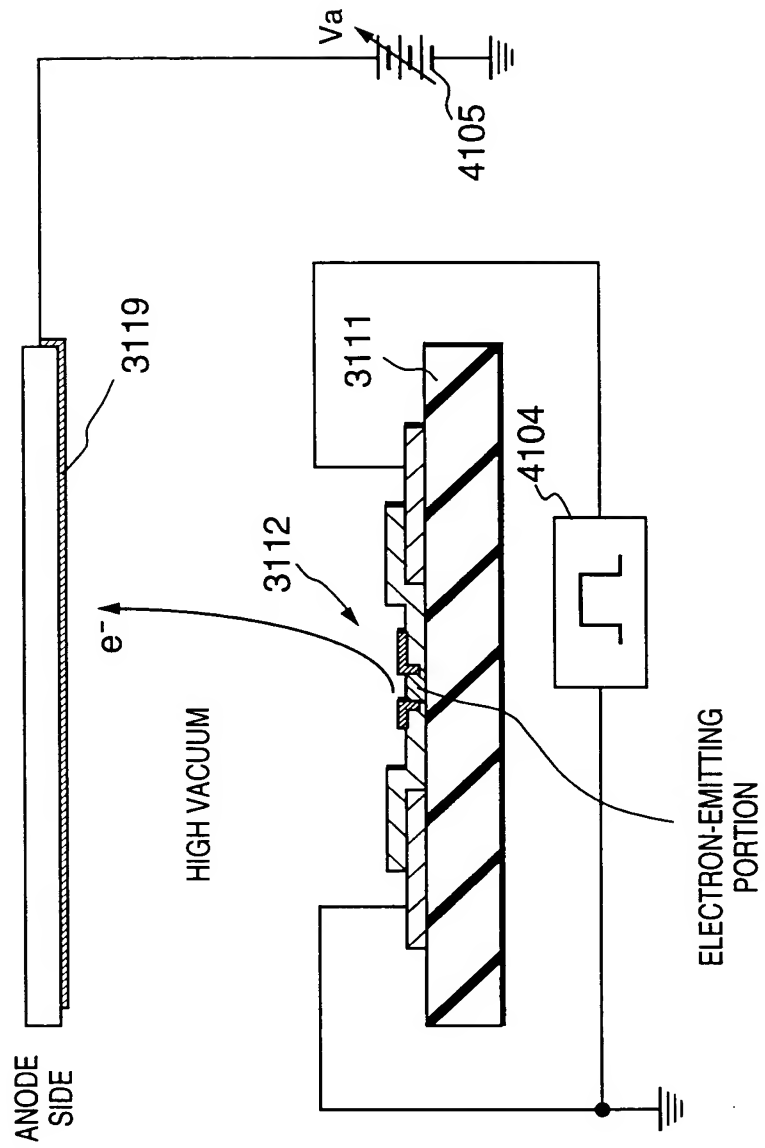






FIG. 34

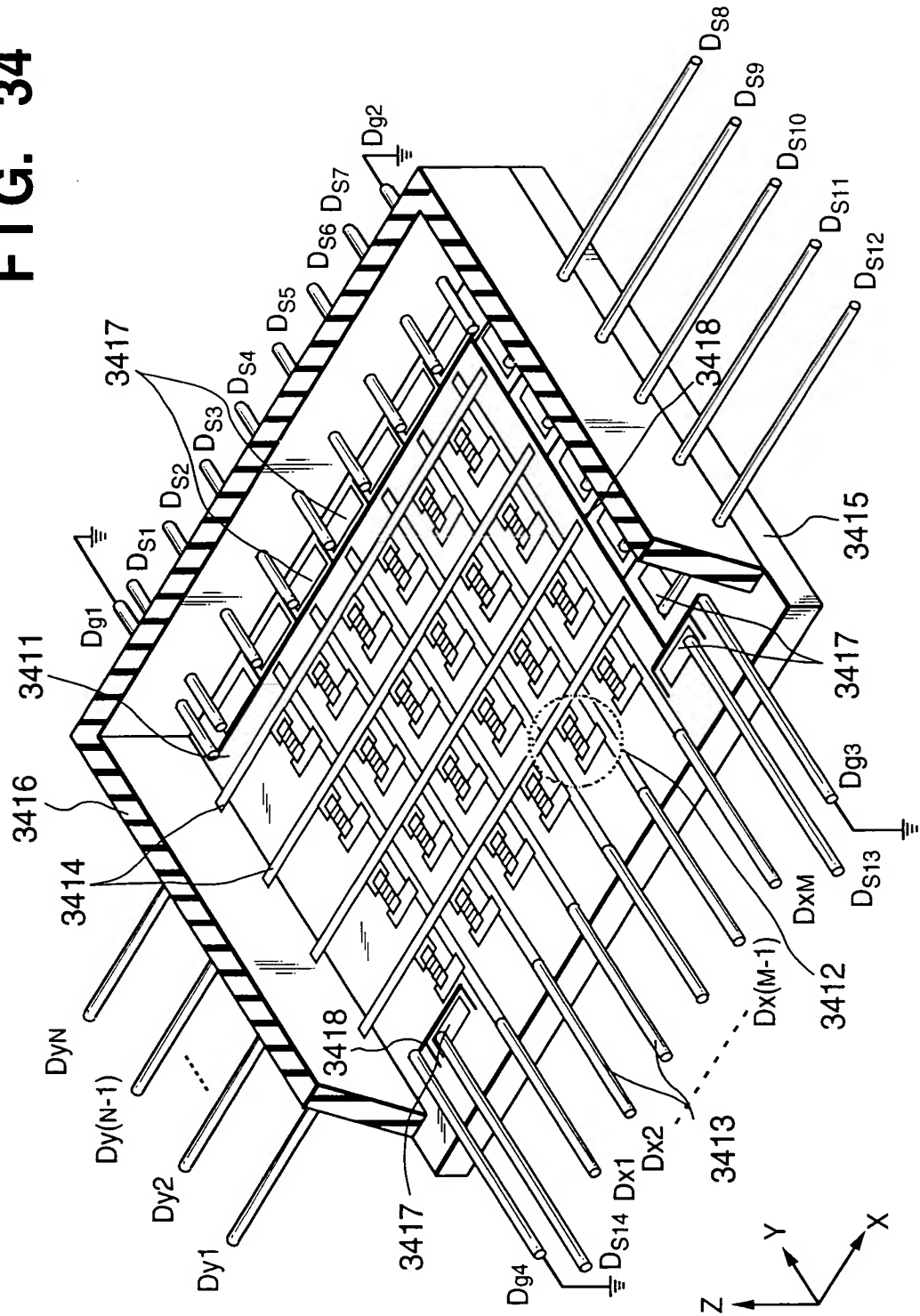


FIG. 35

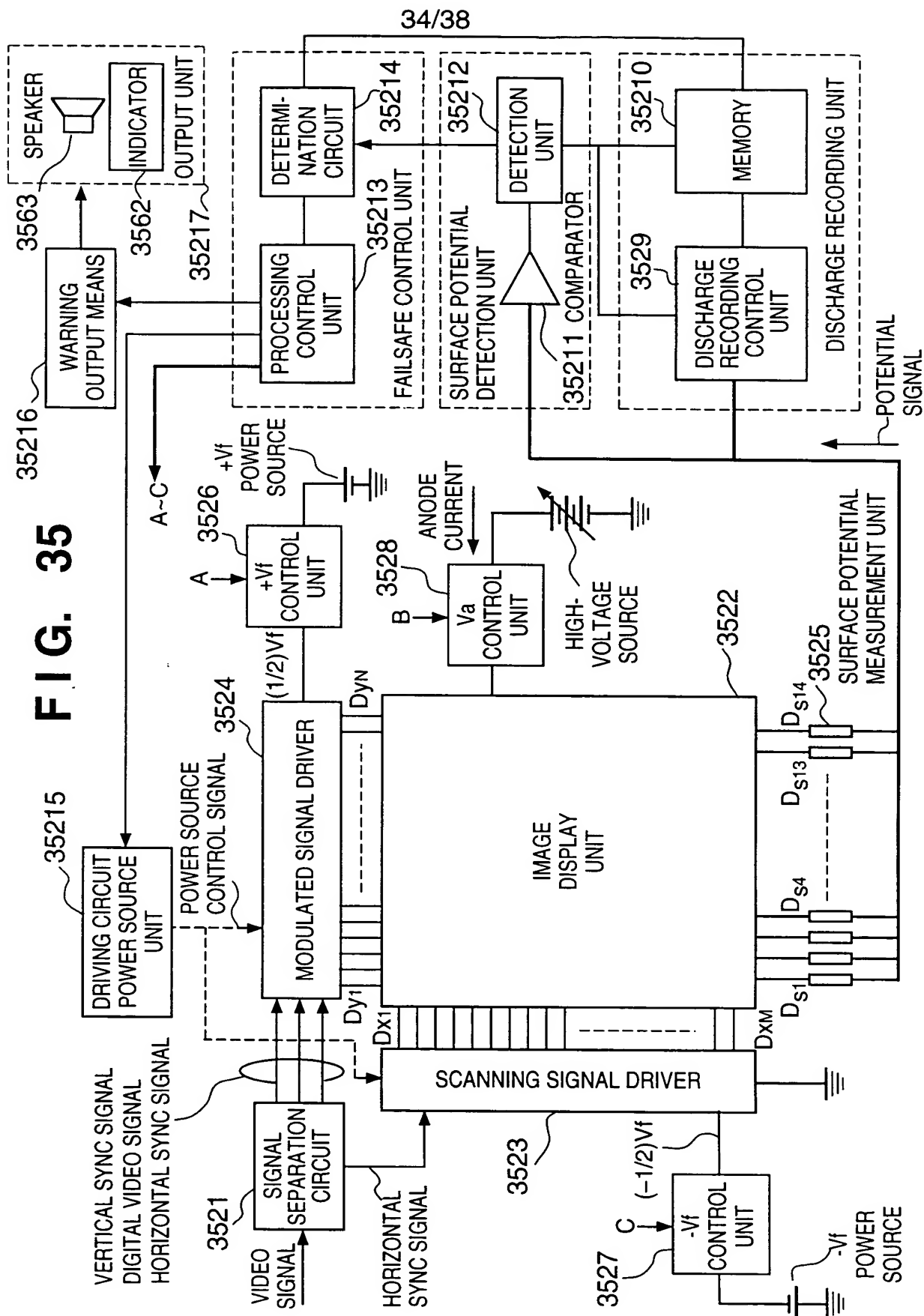


FIG. 36

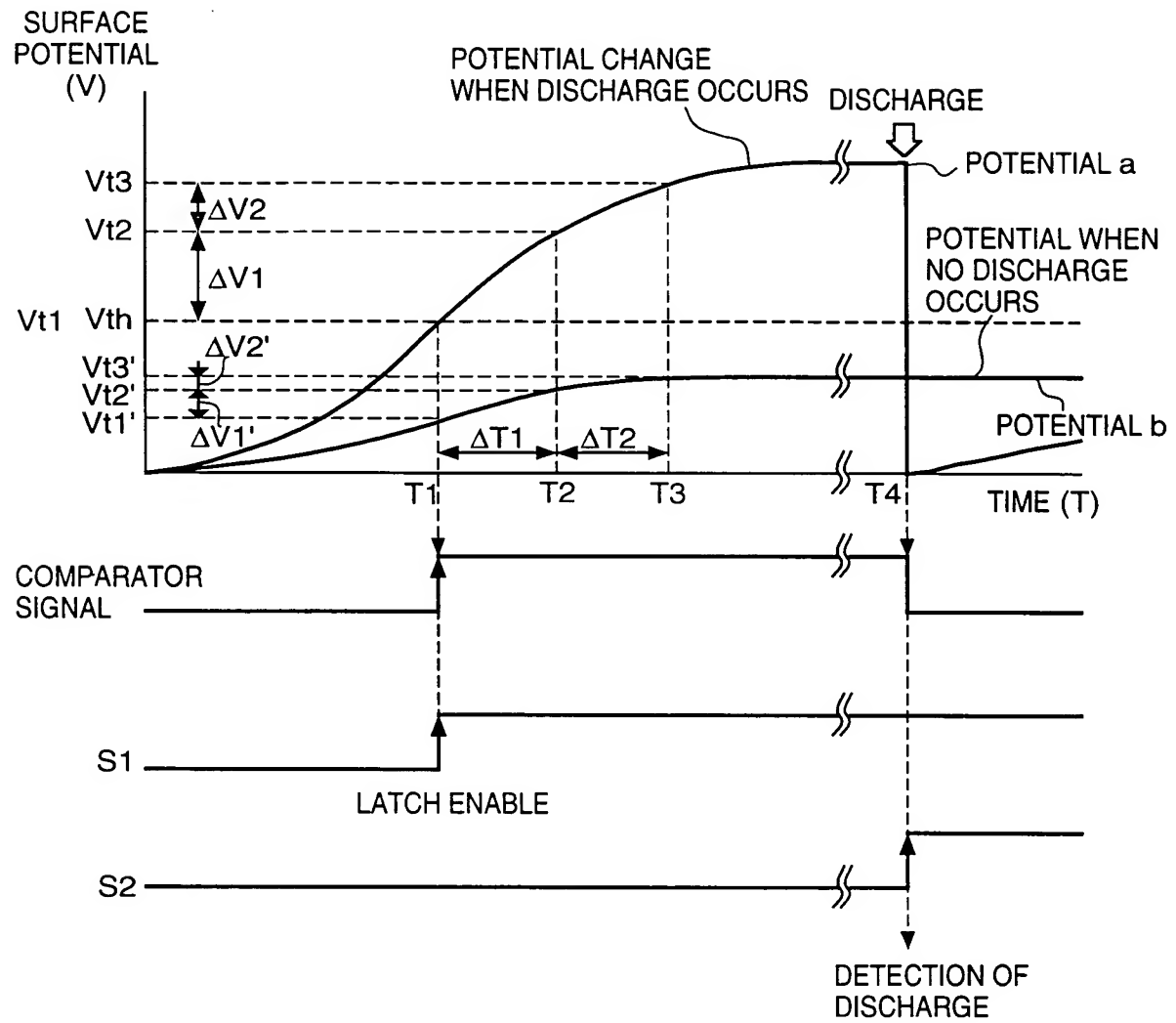


FIG. 37

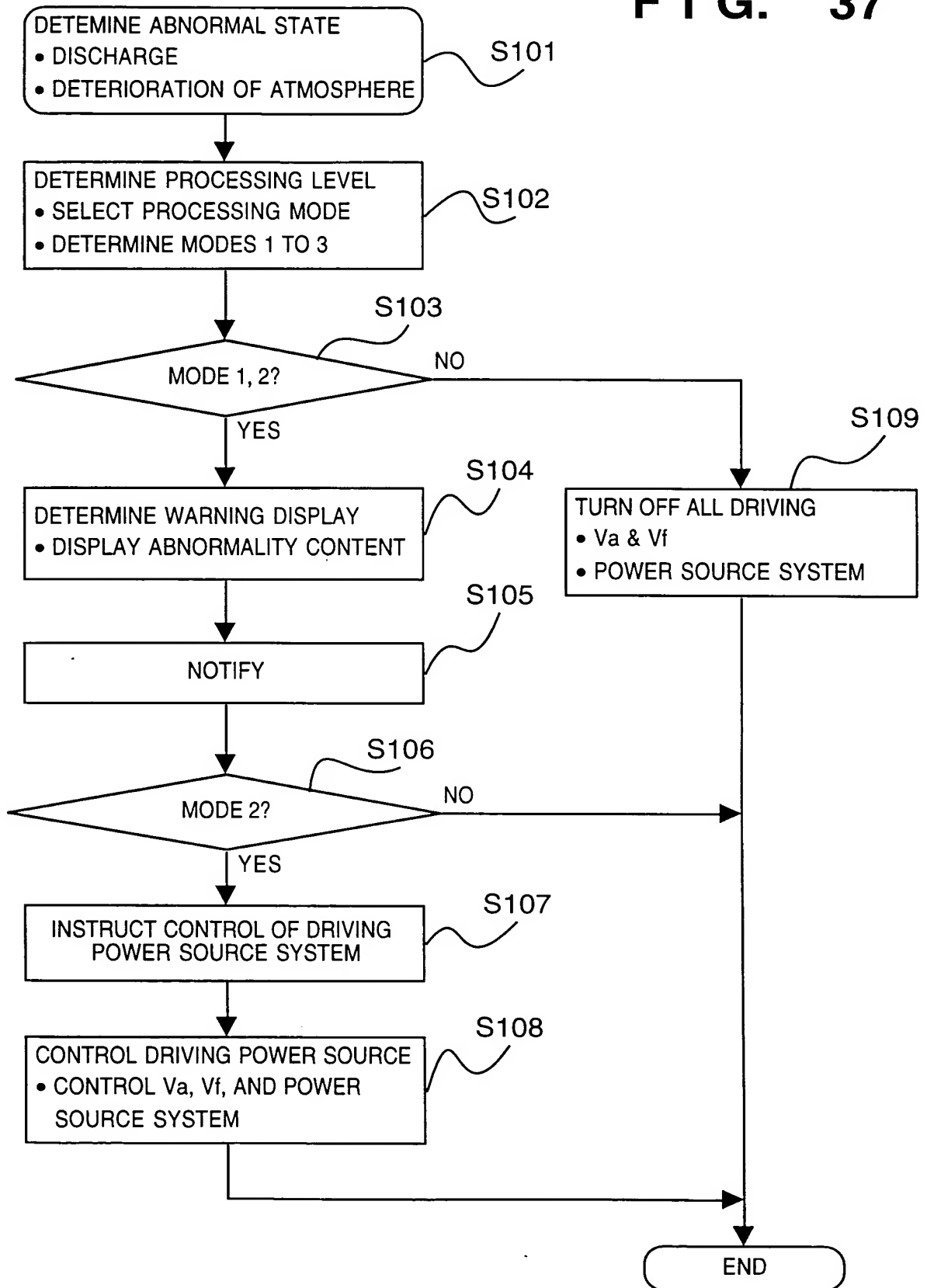


FIG. 38

